User Manual

Tektronix

73A-455
MIL-STD-1553A/B Bus Simulator Module

070-9136-02

This document applies for firmware version 1.00
and above.

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EC Declaration of Conformity

We

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The Netherlands

declare under sole responsibility that the

73A-455 and all options

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

To ensure compliance with EMC requirements only high quality shielded cables having a reliable, continuous outer shield (braid & foil) which has low impedance connections to shielded connector housings at both ends should be connected to this product.

ERROR CODES

The ERR LED is lit when the module detects a syntax error. The E command returns one of the following 2-digit syntax error codes in response to the next input request:

00	No error
01	Unrecognizable command
02	Command line too long
03	Memory full
04	Invalid A (Accept) command
05	Invalid B (Buffer) command
06	Invalid C (Condition) command
07	Invalid D (Data) command
08	Invalid E (Error) command
09	Invalid F (Function) command
10	Invalid G (Gap) command
11	Invalid I (Interrupt) command
12	Invalid M (Error Mode) command
13	Invalid P (Pattern) command
14	Invalid Q (Quit) command
15	Invalid R (Response Time) command
16	Invalid S (Sequence) command
17	Invalid T (Trigger) command
18	Invalid V (Voltage) command
19	Invalid input request

The 73A-455 Module allows several types of errors to be generated to provide for worst-case testing of 1553 bus devices. In addition, errors associated with the 1553 bus can be detected, classified, and stored.

Error Generation

Two different modes of error generation are provided by the M command. Error generation in each mode occurs on an individual word basis. See p. 30 for a listing of the types of errors that can be generated in each mode.

Error Detection

See p. 32 for a listing of the error types detected by the 73A-455, their decimal assignment, and definitions.

73A-455 MIL-STD-1553A/B BUS SIMULATOR MODULE QUICK REFERENCE GUIDE

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 4)
Follow installation guidelines. (p. 17)

The default condition of the 73A-455 Module after the power-up self test is:

- Interrupt: Disabled (I command)
- Transmit Level: 6.38V ptp (VT command)
- Equivalent Bus Load for Transmit Level: 70 ohms (VT command)
- Receive Threshold: 2.00V ptp (VR command)
- Response Gap: 4 µs (R command)
- Pace Interval: 1,000 µs (S command)
- RT Response Time test value: 12 µs (G command)
- Mode: Undefined (F command)
- Pattern Trigger: Disabled (P command)
- Error Mode: Primary error set selected (M command)
- RT Response Time List: Unallocated (B command)
- Sequence List: Unallocated (B command)
- Transmit and Receive Buffers: Unallocated (B command)
- High Speed Mode: Enabled (H command)
- Transition Time Error Detection: Enabled (J command)
- Request True interrupts disabled (these interrupts cause an SRQ on IEEE-488 systems)

LEDs

When lit, the LEDs indicate the following:

Power	power supplies functioning
Failed	module failure
ERR	a syntax error has been found in data received from the system controller
MSG	module is processing a VMEbus cycle
COMM	module has been triggered to begin communication on the 1553 bus
CTRL	channel is programmed to be in the Bus Controller Simulator mode
TERM	channel is programmed to be in the RT Simulator mode
MON	channel is programmed to be in the Bus Monitor mode
PATT	lights immediately after a T command. If a P command was previously issued, it lights when the command or status word pattern specified by the P command is received from the 1553 bus.

SYSTEM COMMANDS

These non-data commands are initiated by the 73A-455's commander. The following VXIbus Instrument Protocol commands will affect the 73A-455:

BEGIN NORMAL OPERATION	CLEAR
BYTE AVAILABLE	READ PROTOCOL
BYTE REQUEST	TRIGGER

COMMAND SYNTAX

Command protocol and syntax for the 73A-455 Module is as follows: (36)

1) If a character is not enclosed by brackets, that character itself is sent, otherwise:
   [] encloses the symbol for the actual argument.
   <CR> = carriage-return; <LF> = line-feed.
2) All characters must be sent in upper case form.
3) Each command consists of a single line of up to 240 characters. Parameters may not be "wrapped around".
4) Every command must end with a <CR>. <LF>s are optional.
5) Use consecutive commas to denote a parameter to be skipped, left at its previous value, or to have its default value accepted.
6) This module does not accept superfluous spaces.

OPERATING MODES

Command order is significant. Refer to the Command Overview (p. 21) for a full discussion of each mode's command set and the required order of commands. Commands available for use in each of the modes, in recommended programming order, are:

Bus Controller	Remote Terminal	Bus Monitor
K	K	K
H (Optional)	H (Optional)	H (Optional)
F	F	F
J (Optional)	J (Optional)	J (Optional)
B	B	M (Optional)
S	R (Optional)	P (Optional)
D	D	V (Optional)
M (Optional)	M (Optional)	T
V (Optional)	P (Optional)	Q
G (Optional)	V (Optional)	C (Optional)
T	T	A (Optional)
Q (Optional)	Q (Optional)	
C (Optional)	C (Optional)	
A (Optional)	A (Optional)	

The following commands are available in every mode: E, H, I, J, K.

Commands

Az_1,z_2,z_3 specifies the data the 73A-455 is to pass back to the system controller in response to the next input request, and the format for this data. (37)

Bz_1,z_2 allocates 73A-455 Module buffers. (42)

Cz examine all data stored in the 73A-455's memory for a given RT buffer, on a block-by-block basis, to find errors in any message block. (45)

$Dz_1,z_2,z_3,z_4,...$ specifies the data list for any one of the 32 transmit buffers in the Bus Controller or Remote Terminal modes. (46)

E instructs the 73A-455 to return the 2-digit syntax error code as a response to the next input request to the 73A-455 Module. (51)

Fz selects bus controller simulator, RT simulator, or bus monitor mode. (52)

Gz specifies the time in µs used to check each RT's response time. (53)

Hz optimizes the execution time of the F, D, T, and A commands. (54)

Iz enables interrupts from the 73A-455 Module. (55)

Jz disables transition time error detection by the 73A-455's receiver. (56)

K returns the 73A-455 to its power-up conditions. (57)

Mz selects one of two different sets of transmitted error conditions. (58)

Pz (optional, only in RT Simulator and Bus Monitor modes), used to program a pattern-recognition word. (59)

Q allows the system controller to terminate a bus communications sequence at any time. It also allows the ATE system controller to regain control of a 73A-455 Module that cannot finish its bus communication sequence because the unit under test (UUT) is not communicating with the 73A-455 Module. (60)

$Rz_1,z_2;z_2;...z_2$ (optional, only in RT Simulator mode) associates a specific RT response time with each message received by the 73A-455 Module. (61)

$Sz_1,z_2[,z_3];z_2[,z_3];...z_2[,z_3]$ used in the Bus Controller Simulator Mode ONLY. Specifies the order in which transmit buffers will send their messages. (65)

$Tz_1[,z_2]$ initiates a 1553 bus communications sequence. (65)

$Vz_1[,z_2]$ programs the 73A-455's peak-to-peak transmit voltage level and receive voltage threshold level. (68)

TEST initiates the self test of PROM and RAM memory. (71)

Table of Contents

Appendices

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Avoid Electric Overload

To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Ground the Product

This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product

Use Proper Power Source

Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:

DANGER
High Voltage

Protective Ground
(Earth) Terminal

ATTENTION
Refer to
Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

73A-455 MIL-STD-1553A/B BUS SIMULATOR MODULE DESCRIPTION

INTRODUCTION

The 73A-455 Module is a printed circuit board assembly for use in a card cage conforming to the VXIbus Specification, such as the 73A-021 used in the CDS 73A IAC System. It allows the system controller in an ATE system to communicate with and test devices that conform to the MIL-STD-1553A/B data bus now being used in many military aircraft and communications systems.

The 73A-455 Module consists of two identical VXIbus instruments in a single-slot VXIbus C-size package. Each of the two separate and independent channels, labeled A and B, has its own VXIbus logical address, its own interrupt, and a complete set of controls and indicators.

NOTE: Each channel of the 73A-455 is truly an independent instrument. Therefore, not only must each separate channel be completely programmed, but all switches on each channel must be properly set. Failure to do so could affect the proper operation of the 73A-455. In addition, the user should pay close attention to proper wiring if any of the 73A-455's auxiliary inputs and outputs are used.

Since each channel must be individually programmed, the descriptions in this manual should be taken to apply to either channel of the module. For example, one of the channels could be set to the 1553 Bus Controller Simulator mode of operation, and the other to 1553 Bus Monitor mode operation.

The 73A-455 Module offers three modes of operation for each channel:

- 1553 Bus Controller (BC) Simulator
- 1553 single or multiple Remote Terminal (RT) Simulator
- 1553 Bus Monitor

In the Bus Controller Simulator mode, each channel of the 73A-455 has the ability to communicate with any or all of the 32 remote terminals (31 real devices plus broadcast mode) specified by MIL-STD-1553A/B. Each channel is loaded by the system controller with a bus controller message sequence list and data lists for each RT to be addressed. When instructed to do so by the system controller, the selected 73A-455 channel transmits pre-programmed messages to the respective RT(s). Any response data received from the RT is stored in on-card memory for that channel.

In the RT Simulator mode, each channel of the 73A-455 Module can simultaneously emulate any or all of the different RTs. The system controller preloads the 73A-455 with the appropriate response data and status words for each simulated RT. Data received from the 1553 bus by the 73A-455 is stored in on-card memory for that channel for later evaluation.

In the Bus Monitor mode, the selected channel of the 73A-455 Module assumes an essentially passive role; it simply observes and stores all bus traffic. Up to 30,000 data, command, or status words can be

stored in channel memory for later evaluation.

The 73A-455 allows introducing controlled errors into the transmitted data stream for each channel to provide worst-case testing of 1553 bus devices. These errors include incorrect parity, erroneous 1553 Manchester encoding, zero crossing errors of ±150 ns, dropped data bits, interword data gaps, incorrect or invalid 1553 sync patterns, incorrect RT response times, incorrect number of data bits per word, incorrect number of words per message, invalid signal levels, and common-mode signal injection.

On received data, the 73A-455 Module can distinguish between incorrect transition time errors, Manchester errors, dropped data-bit errors, bit count errors, parity errors, incorrect sync errors, terminal response time errors, interword data-gap errors, word count errors, and message format errors such as incorrect RT address, missing RT response, invalid status words, invalid mode code usage, and invalid broadcast mode usage.

The 73A-455 Module self test capability is programmable with a single command. Each channel is tested independently.

Each channel of the module is programmed by sending ASCII characters to the 73A System from the system controller. Data is also returned to the system controller as ASCII characters.

Depending on the context, the two components of the 73A-455 may be referred to in this manual as VXIbus instruments, module channels A and B, or 1553 channels.

Note that certain terms used in this manual have very specific meanings in the context of a VXIbus System. A list of these terms is presented in the VXIbus Glossary (Appendix C).

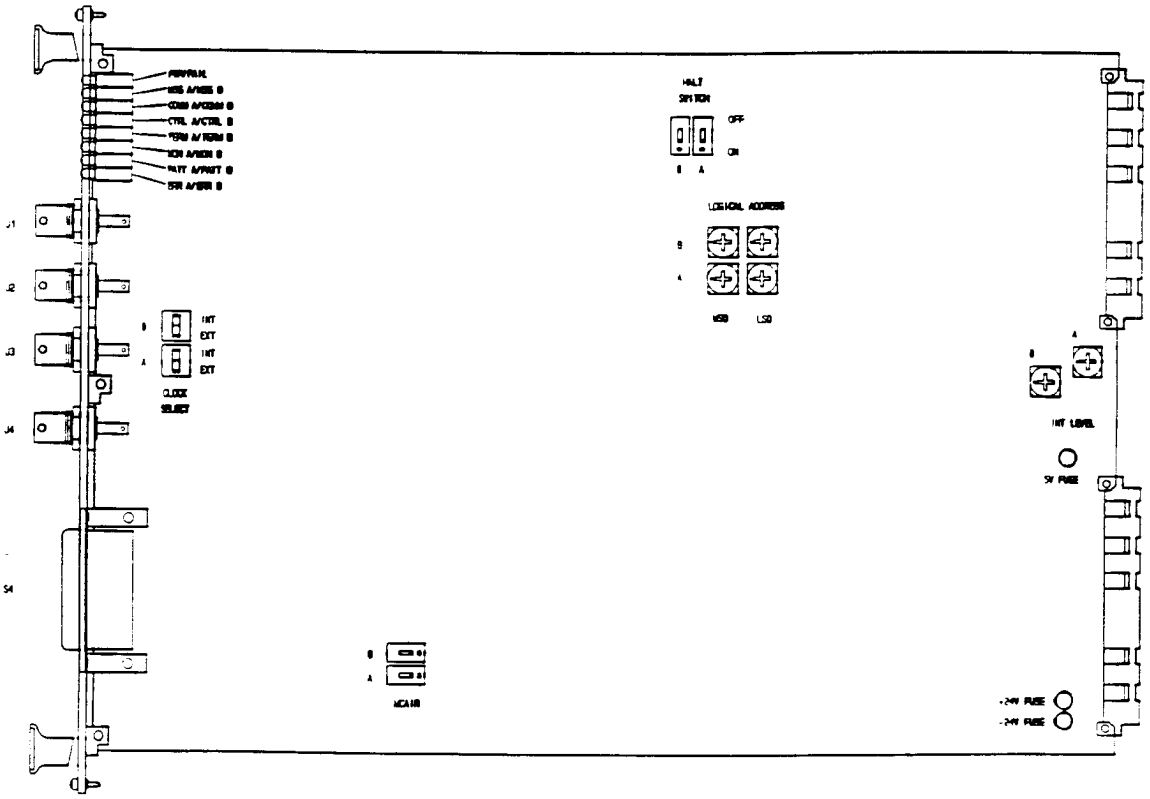


Figure 455-1: 73A-455 Controls and Indicators

CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 73A-455 Module's operating environment. See Figure 455-1 for their physical locations.

NOTE: Each channel of the module has a complete and separate set of controls and indicators. The switches and controls for the "A" channel (connected to the output connectors labeled "A" on the front panel) are connected to the bottom board and are furthest away from the shield when the module is viewed from the component side.

- **Switches**

Logical Address Switches

Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 254 decimal. The base VMEbus address of each channel of the 73A-455 is set to a value between 1 and FEh (254d) by two hexadecimal rotary switches. There are two sets of these switches, one for each channel, located in the upper rear quadrant of the module.

CAUTION:

The two logical channels that comprise the 73A-455 should never be assigned the same logical address. In an IEEE-488 application, if you override the IEEE-488 address assigned by the slot 0 module, do not assign the same address to the two channels.

The actual physical address of each channel of the 73A-455 module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the channel will be [(64d * XYh) + 49152d]. For example:

L.A.	M S D	L S D	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the 73A-455 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the 73A-455 is being used in a CDS IEEE-488 IAC system, consult the operating manual of the CDS 73A-1XX Series slot 0 embedded controller or IEEE-488 Interface Module.

If the 73A-455 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC). This algorithm is described in detail in the 73A-156 Operating Manual.

If the 73A-455 is not being used in a CDS IAC System, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the module's logical address(es).

VMEbus Interrupt Level Select Switch

Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander (for example, the 73A-151B RM/IEEE-488 Interface module in a CDS 73A-IBX System). The VMEbus interrupt level on which a given channel of the 73A-455 Module generates interrupts is set by one of two BCD rotary switches located at the center rear of the module. Align the desired switch position for each channel to the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the interrupt handler for each channel of the 73A-455, typically the module's commander. Setting the switch to an invalid interrupt level (0, 8, or 9) will disable the module's interrupts.

When using the 73A-455 in a CDS 73A-IBX System, set the interrupt level for each channel to the same level chosen for the 73A-151.

If the 73A-455 is being used as part of a 73S-456 MIL-STD-1553A/B Bus Tester Instrument Set, consult the 73S-456 Operating Manual for information on setting the switch for each channel.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

Halt Switch

These two-position slide switches, located near the top rear of the module, select the response for each channel of the 73A-455 Module when the Reset bit in the module's VXIbus Control register is set.

If the Halt switch is in the ON position, then that channel of the 73A-455 Module is reset to its power-up state and all programmed parameters for that channel are reset to their default values.

If the Halt switch is in the OFF position, that channel will ignore the Reset bit and no action will take place.

NOTE: The module (or channel) is not in strict compliance with the VXIbus Specification when the Halt switch for that channel is in the OFF position.

Control of the Reset bit depends on the capabilities of the 73A-455's commander. In a CDS 73A-IBX System, for example, the Reset bit is set if the 73A-151 RM/IEEE-488 Interface Module receives a STOP command through the IEEE-488 bus.

Clock Select Switch

These two-position rocker switches are located on the side of the module near the center front. They select either internal or external data clock for a channel of the module. In the INT position, the internal data clock is selected, and the 1553 bus data rate is 1 MHz. When the switch is in the EXT position, an external 16-MHz data clock is selected. The external clock can be varied over the frequency range of 15 MHz to 17 MHz, allowing the 1553 bus data rate to be varied from 937.5 KHz to 1.0625 MHz.

MAC Air Switch

These slide switches are located on the side of the module near the bottom edge. When a channel's switch is in the OFF position, the rise and fall times of data generated by that channel of the 73A-455 Module will be between 150 and 250 nanoseconds with two 70-ohm bus terminations. When the switch is in the ON position, the rise and fall times

of generated data will be between 220 and 350 nanoseconds with two 70-ohm bus terminations.

- **Fuses**

The 73A-455 Module has fuses for +5V, +24V, and -24V. The fuses protect the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

Each of the three fuses is shared by both instruments in the 73A-455. The +24V and −24V fuses are 2A socketed fuses. The +5V fuse is a 7A soldered fuse.

If the +5V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If a fuse opens, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section of this manual.

- **LEDs**

The following LEDs are visible at the top of the 73A-455 Module's front panel to indicate the status of the module's operation. See Figure 455-2.

The PWR and FAIL LEDs indicate the status of the entire 73A-455 Module. The remaining LEDs indicate the status of either Bus A or Bus B.

PWR LED

This green LED is normally lit and is extinguished when the +5 volt, ±24 volt, or internal ±15 volt power supplies fail.

FAIL LED

This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure due to loss of a power rail.

NOTE: If the module loses any of its power voltages, the FAIL LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's PWR LED is extinguished.

The 73A-455 Module has two of all of the following LEDs located on its front panel, one for the "A" channel and one for the "B" channel. Since the two channels are identical and separate, the descriptions for each LED apply equally to both channels.

MSG LED

This green LED is normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

COMM LED

The COMM LED lights when the 73A-455 Module has been triggered to begin communication on the 1553 bus. When not lit, it indicates that the 73A-455 Module is available for data or command transactions with the ATE system controller.

Function LEDs

Three function LEDs indicate which mode of operation has been selected for the channel. The CTRL LED is lit when the card is programmed to be in the Bus Controller Simulator mode, the TERM LED is lit for RT Simulator mode, and the MON LED is lit for the Bus Monitor mode.

PATT LED

The PATT LED will light immediately after a T command has been issued unless a P command was previously issued to the 73A-455 Module; in this case, it will light when the command or status word pattern specified by the P command is received from the 1553 bus.

ERR LED

This amber LED lights whenever the 73A-455 Module detects a syntax error in the data received from the system controller. After the system controller interrogates the error (with an E command), the light will go out. This LED is typically used as a debugging aid during software development.

BITE (Built-In-Test Equipment)

The TEST command (see Operation section) provides a complete RAM and ROM self test for each channel. In addition, the front panel LEDs light in sequence to provide visual indication of the test in progress.

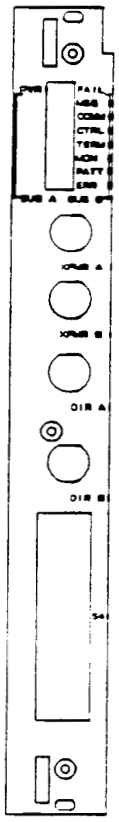


Figure 455-2: Front Panel

GLOSSARY

A glossary of VXIbus terms is provided in Appendix C. In addition, the following terms specific to the 73A-455 Module are defined:

Bus Communications Sequence

The 73A-455 Module is said to be performing a Bus Communications Sequence during the time the card is transmitting or receiving data over the 1553 data bus. A Bus Communications Sequence is initiated when the 73A-455 receives a T (Trigger) command from the system controller.

In the Bus Controller Simulator mode, a Bus Communications Sequence is completed when all messages specified by the Bus Controller Sequence List have been transmitted the number of times required by the T command.

In the RT Simulator mode, a Bus Communications Sequence is completed when the total number of messages specified by the T command have been received.

In the Bus Monitor mode, the Bus Communications Sequence is completed when a Q command or an External Halt Input is received by the 73A-455.

Bus Controller

The single device attached to the 1553 data bus that is assigned the task of initiating information transfers on the bus.

Bus Controller Sequence List

This list specifies the order in which messages are transmitted in the Bus Controller Simulator mode.

Command Word

A 16-bit word sent by the bus controller to identify or address the RT to be involved in a bus transaction. It also specifies whether the terminal will be transmitting or receiving data.

Data List

An individual data list may be defined for each of the transmit buffers (up to 32) provided on each channel of the 73A-455 Module. When the module is in the Bus Controller Simulator mode, an individual data list contains the command and data words to be sent from a specific buffer. When the module is in the RT Simulator mode, an individual data list contains the status and data words a simulated RT will return to the bus controller.

Data Word

A 16-bit word containing the actual data in a 1553 bus transaction.

Message or Message Block

The combined transaction (command, status, and data) associated with one command word.

Remote Terminal (RT)

One of up to 31 devices connected to the 1553 data bus that is capable of sending data to or receiving data from the bus controller.

RT Response Time List

When the 73A-455 Module functions as an RT simulator, the card is preloaded with a list of RT response times to be used when responding to each command word received from the bus controller. RT response time values are used from the RT Response Time List in sequential order, regardless of the RT numbers addressed by the incoming command words.

RT Response Time or Response Time Gap

The response time of an RT is the time in microseconds between the middle transition of the parity bit of the last command or data word received by the RT and the middle transition of the sync pattern in the status word transmitted by the RT.

Status Word

A 16-bit word returned by an RT after being addressed by the bus controller.

System Controller

The test system computer providing control and data information to the 73A System via a suitable communications link (IEEE-488, etc.)

Word

A 1553 word is a sequence of 20 bit-times consisting of a sync pattern of three bit-times, followed by 16 bits of data and one bit of parity. Though each word is 20 bit-times in length, a word contains only 16 bits of data and is commonly referred to as a 16-bit word. The three types of 1553 words are: command words, status words, and data words.

SPECIFICATIONS

Instrument Specifications

These specifications apply equally to both the "A" and "B" instrument channels.

Configuration:	MIL-STD-1553 Bus Controller Simulator, single or multiple RT Simulator, or Bus Monitor.
1553 Bus Coupling:	
Direct Coupling:	1:1 turns ratio, 55-ohm isolation resistor each leg.
Transformer Stub Coupling:	1:0.707 turns ratio.
Operating Modes:	
Bus Controller Simulator:	Programmable for 32 separate data lists.
RT Simulator:	Programmable for data collection and response from 32 separate RT associated buffers.
Bus Monitor:	Collects all data on bus in single buffer, receive-only mode.
Buffer Capability:	30,000 22-bit words - 16 bits data, 6 bits error/sync code. Can be allocated between 32 transmit buffers, 32 receive buffers, and a single Bus Controller Sequence List or RT Response Time List. Allocation is totally user-controlled.
1553 Analog Output:	Level-programmable to approximately 250 different levels.
Range:	Voltage range depends on the bus loading. Differential voltage level output range for the following bus loads is: 35 ohms, direct-coupled output 0.20 to 8.20 V ptp. 70 ohms,direct-coupled output 0.30 to 13.75 V ptp. 1000 ohms, direct-coupled output 0.75 to 34.40 V ptp. 70 ohms, transformer-coupled output, 0.60 to 24.2 V ptp. At 1553 bus with two 70 ohm terminators, either direct-coupled direct connection or transformer-coupled through MIL-STD-1553 coupler. 0.20 to 8.20 V ptp. The above levels are for the MAC Air switch in the OFF position. With the MAC Air switch in the ON position, the peak-to-peak levels are approximately 10% higher than shown.
Accuracy:	±0.3 V ptp with 35 and 70 ohm loads.

Noise Content:	50 mV ptp.
Current Drive:	260 mA RMS maximum, direct-coupled output. 380 mA RMS maximum, transformer-coupled output.
Short-circuit Protection:	The direct-coupled output may be shorted for several minutes without degradation of the transmitter. The transformer-coupled output should not be shorted. Shorting may cause damage to the module.
1553 Analog Input:	
Maximum Input:	40 V ptp differential.
Threshold:	Programmable to approximately 250 different levels. Programmable from 0.50 to 9.00 V ptp at direct-coupled input (equivalent to 0.35 to 6.36 V ptp at transformer-coupled input).
Transition Time Error Detection:	Time from one threshold crossing to the next threshold crossing is nominally expected to be 0.5, 1.0, 1.5 or 2.0 microseconds, per MIL-STD-1553. The receiver checks that this time is reliably within 62.5 nanoseconds of the nominally expected time.
Word Format:	Manchester bi-phase, self-clocking, 1 MHz, 20-bit word with command/data sync, data, and parity bits, per MIL-STD-1553A/B.
Message Format:	Programmable command or status word plus user-defined number of data words per message.
Message Capability:	Any number of messages may be specified for transmittal or receipt, subject only to a constraint on available buffer memory (30,000 words). A message requires one word of buffer memory for each command, status, or data word transmitted or received. In the Bus Controller Simulator mode, two additional words per message are required for system overhead.
Message Rate:	
Bus Controller Simulator Mode:	(Time from the end of one message to the start of the next message). Programmable from 14 microseconds to 65,535 microseconds on an individual message basis.
RT Simulator Mode:	(RT response time) Programmable from 4.25 microseconds to 65,535.25 microseconds on an individual message basis.

Bus Monitor Mode:	Message rate is defined by active devices on bus.
Message Synchronization:	The start of an RT operation in the RT Simulator mode or the start of data collection in the Bus Monitor mode may be programmed to start on a user-specified pattern word received from the 1553 bus controller.
Induced Transmitter Errors:	Programmable on an individual word basis to give incorrect parity, Manchester error, dropped bit error, sync pattern error, or incorrect bit count (±1 bit). By programming a secondary error mode, programmable on an individual word basis to give ±150-ns bit transition time error, ±150-ns sync transition time error, dropped parity bit, or 1-bit interword gap error. In addition, programmable on an individual message basis to give incorrect RT response time, word count, or status word RT address. Bit position of Manchester, dropped bit, and transition time errors are controllable as a function of the 16-bit word data content.
Receiver Error Checking:	Detects and distinguishes bit transition time errors, parity errors, dropped bit errors, sync pattern errors, and receiver response time errors on an individual word basis for subsequent return to system controller. The response-time error test value is programmable from 4 to 31 microseconds. Detects interword data gap error, word count errors, no RT response, or incorrect RT address on an individual message basis for return to the system controller. Format errors are also detected for improper mode code operation, improper broadcast mode operation, and improper use of status word bits.
Time Base:	16 MHz crystal oscillator. Optional switch-selectable user clock input on front-edge connector for 16 times desired data rate. Optional clock input from 15 MHz to 17 MHz. Frequency tracking of 0.1% to any other units on the bus must be maintained.
Interrupt Capability:	The module may be programmed to interrupt the system controller on completion of a bus communications sequence.
Programmed By:	ASCII characters. Data is transferred between the system controller and 73A-455 Module using either a hexadecimal or a binary encoded format.
Auxiliary Outputs (TTL levels):	Reconstructed Received Data and Clock. Transmitted Data and Clock. Pattern Recognition Output. Status Error Output.

	Data Word Received Output. Data Bus Input Active Output. Position Identification Output.
Auxiliary Inputs (Analog):	
Common-mode Voltage:	For external injection of common-mode voltage onto 1553 bus.
Maximum Input Rating:	6 V RMS.
Auxiliary Inputs (TTL):	External 1553 Data Rate Clock. External Halt Input. External Trigger Input. External Transmitter Enable Input.
Power Up:	Module is ready for programming 1 second after power-up. Power LED on, all other LEDs off 0.5 seconds after power-up. Default condition on power-up is: Interrupt: Disabled (I command). Transmit Level: 6.38 V ptp (VT command). Equivalent Bus Load for Transmit Level: 70 ohms (VT command). Receive Threshold: 2.00 V ptp (VR command). Response Gap: 4 µs (R command). Pace Interval: 1,000 µs (S command). RT Response Time test value: 12 µs (G command). Mode: Undefined (F command). Pattern Trigger: Disabled (P command). Error Mode: Primary error set selected (M command). RT Response Time List: Unallocated (B command). RT Sequence List: Unallocated (B command). Transmit and Receive Buffers: Unallocated (B command). High Speed Mode: Enabled (H command). Transition Time Error Detection: Enabled (J command). Request True interrupts disabled (these interrupts cause an SRQ on IEEE-488 systems).
VXIbus Compatibility:	Fully compatible with the VXIbus Specification for message-based instruments with the Halt switch in the ON position.
VXI Device Type:	VXI message based instrument, VXIbus Revision 1.2.
VXI Protocol:	Word serial.
VXI Card Size:	C size, one slot wide.
Module-Specific Commands:	All module-specific commands and data are sent via the VXIbus Byte-Available command. All module-specific

commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.

VMEbus Interface: Data transfer bus (DTB) slave - A16, D16 only.

Interrupt Level: Switch selectable, levels 1 (highest priority) through 7 (lowest).

Interrupt Acknowledge: D16, lower 8 bits returned are the logical address of the module.

VXIbus Commands Supported: All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command event:

BYTE AVAILABLE (with or without END bit set)
BYTE REQUEST
BEGIN NORMAL OPERATION
READ PROTOCOL
CLEAR
TRIGGER

VXIbus Protocol Events Supported: VXIbus events are returned via VME interrupts. The following events are supported:

UNRECOGNIZED COMMAND
REQUEST TRUE (This interrupt will cause IEEE 488 interface devices to assert SRQ [service request]).

VXIbus Registers:
ID
Device Type
Status
Control
Protocol
Response
Data Low
See Appendix A for definition of register contents.

Device Type Register Contents: FE38h (1s complement of binary value of model number).

System Specifications

These specifications apply to the complete 73A-455 Module.

Power Requirements: All required dc power is provided by the Power Supply in the VXIbus card cage.

Voltage:	+5 Volt Supply:	4.75 V dc to 5.25 V dc.
	+24 Volt Supply:	+23.2 V dc to +25.2 V dc.
	-24 Volt Supply:	-23.2 V dc to -25.2 V dc.

Current (Peak Module, I_{PM}):	5 volt supply:	5 A
	+24 volt supply:	0.4 A
	-24 volt supply:	0.4 A
Current (Dynamic Module, I_{DM}):	5 volt supply:	0.05 A
	+24 volt supply:	0.2 A
	-24 volt supply:	0.2 A

Cooling: Provided by the fan in the VXIbus card cage. Less than 10°C temperature rise with 1.1 liters/sec of air at a pressure drop of 0.02 mm of H_2O.

Temperature: -10°C to +65°C, operating (assumes ambient temperature of 55° and airflow to assure less than 10°C temperature rise).
-40°C to +85°C, storage.

Humidity: Less than 95% R.H. non-condensing, -10°C to +30°C.
Less than 75% R.H. non-condensing, +31°C to +40°C.
Less than 45% R.H. non-condensing, +41°C to +55°C.

VXI Bus Radiated Emissions: Complies with VXIbus Specification.

VXI Bus Conducted Emissions: Complies with VXIbus Specification.

Module Envelope Dimensions: 262 mm high, 352 mm deep, 31 mm wide.
(10.3 in x 13.9 in x 1.2 in).

Dimensions, Shipping: When ordered with a CDS card cage, this module will be installed and secured in one of the instrument module slots (slots 1 - 12).

When ordered alone, the module's shipping dimensions are:

406 mm x 305 mm x 102 mm. (16 in x 12 in x 4 in).

Weight: 1.9 kg. (4.1 lb).

Weight, Shipping: When ordered with a CDS card cage, this module will be installed and secured in one of the instrument module slots (slots 1-12).

When ordered alone, the module's shipping weight is:

2.8 kg. (6.0 lb).

Mounting Position: Any orientation.

Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus card cage. (Refer to D size card cage manual for information on required adapters.)
Front Panel Signal Connectors:	4 - TNC Triax female connectors or DD50S for optional signals. Refer to Appendix B for connector pinouts.
Equipment Supplied:	1 - 73A-455 Module.
Optional Equipment:	1 - 73A-780P Hooded Connector for connection to DD50S connector.

INSTALLATION

INSTALLATION REQUIREMENTS AND CAUTIONS

The 73A-455 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus card cage slot other than slot 0. If the module is being installed in a D size card cage, consult the operating manual for the card cage to determine how to install the module in that particular card cage. Setting the module's two Logical Address switches defines the programming addresses of the two instruments in this module. Refer to the Controls and Indicators subsection for information on selecting and setting the 73A-455 Module's logical address.

Tools Required:

The following tools are required for proper installation:

Slotted screwdriver set.

CAUTION:

Note that there are two ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector labeled "73A-455" is at the top.

CAUTION:

In order to maintain proper card cage cooling, unused card cage slots must be covered with blank front panels supplied by the card cage manufacturer. Based on the number of IAC Modules ordered with a CDS card cage, blank front panels are supplied to cover all unused slots.

CAUTION:

Verify that the card cage is able to provide adequate cooling and power for the 73A-455 Module. Refer to the card cage Operating Manual for instructions on determining cooling and power compatibility.

CAUTION:

If the 73A-455 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the 73A-455 Module to operate properly. Check the manual of the card cage being used for jumpering instructions.

If a CDS 73A-021 Card Cage is being used, the jumper points may be reached through the front of the card cage. There are five jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

INSTALLATION PROCEDURE

CAUTION:

The 73A-455 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the module's Revision Level, Serial Number (located on the CDS label on the top shield of the 73A-455), and switch settings on the Installation Checklist on the next page. Only qualified personnel should install the 73A-455 Module.

2) Verify that the Logical Address and Interrupt Level switches are switched to the correct value for each channel. The two Halt switches should be in the ON position unless it is desired to not allow the resource manager to reset this module.

   Note that with either Halt switch position, a "hard" reset will occur at power on and when SYSRST* is set true on the VXIbus backplane. If the Module's commander is a CDS 73A-151 RM/IEEE-488 Interface Module, SYSRST* will be set true whenever the Reset switch on the front panel of the 73A-151 is depressed. Also note that when the Halt switch is in the OFF position, the operation of this module is not VXIbus compatible.

3) The module can now be inserted into any slot of the chassis other than slot 0. Fasten the module to the card cage with the captive screws in the module front panel.

4) Four TNC Triax female connectors are provided at the top of the front panel. XFMR A and XFMR B are for transformer-coupled connections to the MIL-STD-1553 Bus A and B, and DIR A and DIR B for direct-coupled connection to the MIL-STD-1553 Bus A and B. Install a cabled TNC Triax male connector to one of the two connector sets.

   Use a 73A-782S Hooded Connector to provide the interface to any of the optional I/O signals available on the DD50P connector labeled S4. It is recommended that you wire only those signals to be used. The transformer- and direct-coupled MIL-STD-1553 bus connections are also available on the DD50P connector as an alternative to the triax connectors.

   If the module is being installed in a CDS 73A Series card cage, route cables from the front panel of the module down through the cable tray at the bottom of the card cage and out the rear of the card cage.

INSTALLATION CHECKLIST

Installation parameters may vary depending on the card cage being used. Be sure to consult the card cage Operating Manual before installing and operating the 73A-455 Module.

Revision Level: _____

Serial No.: _____

Card Cage Slot Number: _____

Switch Settings, Channel A:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Halt Switch: _____

Clock Select Switch: _____

MAC Air Switch: _____

XFMR A or DIR A Cable Connection Installed: _____

Switch Settings, Channel B:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Halt Switch: _____

Clock Select Switch: _____

MAC Air Switch: _____

XFMR B or DIR B Cable Connection Installed: _____

(optional)
73A-782S Hooded Connector installed (if required): _____

Performed by: _____ Date: _____

OPERATION

OVERVIEW

Each channel of the 73A-455 Module is programmed by ASCII characters issued from the system controller to the 73A-455 Module via the VXIbus card cage backplane.

NOTE: Each of the channels must be programmed separately.

The module is a VXIbus Message Based instrument and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the 73A-455 Module's commander for details on the operation of that device.

If the module is being used in a CDS 73A-IBX System card cage, the module's commander will be the 73A-151 Resource Manager/IEEE-488 Interface Module. Refer to the 73A-151 Operating Manual and the programming examples in the Operation section of this manual for information on how the system controller communicates with the 73A-151.

MIL-STD-1553 provides for time-division multiplexed communication by up to 31 avionics units (RTs) via a two-wire, high-speed, 1-MHz, command/data bus. According to the defined protocol, a single bus controller at any one time controls the flow of information among the RTs. If further information is needed, refer to the standard (MIL-STD-1553B or MIL-HDBK-1553B may be obtained from the Naval Publications Center, Philadelphia, PA, (215) 697-2179 or your in-plant government publication department).

Each channel of the 73A-455 Module can operate in any one of three modes: Bus Controller Simulator mode, RT Simulator mode, or Bus Monitor mode.

For controller-to-RT transactions, a 16-bit command word is sent which specifies the RT that is to receive data, and the number of data words (up to 32) to be received. The RT then processes the command information and the data and returns a 16-bit status word containing the RT address and status information.

For RT-to-controller transactions, the bus controller sends a 16-bit command word specifying the RT address and the number of data words (up to 32) to be transmitted. The RT then returns a status word with its own address and status, followed by the required data transmission.

Each word (command, status, or data) is a 16-bit word encoded in a Manchester bi-phase format that eliminates the need for separate clock lines and minimizes any DC voltage component on the common bus. The 16-bit word is always preceded by a 3-bit-time sync signal and followed by an odd parity bit. The sync signal is defined as being high for 1½ bit-times, then low for 1½ bit-times for a command or status word. This sequence is reversed (low, then high) for a data word.

Additional types of operation providing for RT-to-RT transfers, a set of defined mode codes, and a broadcast mode, are described in MIL-STD-1553B.

POWER-UP

The 73A-455 Module will be ready for programming five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay. The

Power LED will be on, and all other LEDs off. The MSG LED will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the card cage. The default condition of the module after power-up is described in the SYSFAIL, Self Test and Initialization subsection.

SYSTEM COMMANDS

Although these non-data commands are initiated by the 73A-455's commander (for example, the 73A-151 Module in a CDS 73A-IBX System) rather than the system controller, they have an effect on the 73A-455 Module. The following VXIbus Word Serial commands will affect the 73A-455:

Command Effect

Clear
: The module clears its VXIbus interface. Current module operations are unaffected.

Trigger
: The 73A-455 Module will begin operation as a 1553 bus controller, RT or monitor according to the commands that have been sent to it prior to the VXI trigger command. External triggering must be specified by the T command to enable the VXI trigger command.

Begin Normal Operation
: The module will begin operations.

Read Protocol
: The module will return its protocol to its commander.

COMMAND OVERVIEW

This section explains the order of commands, and describes each of the three modes: Bus Controller mode, Remote Terminal mode, and Bus Monitor mode. The mode descriptions give typical examples and are general in nature, intended to indicate some possible uses and to suggest ideas for using the 73A-455 in other applications.

Each command is described in full in the Detailed Descriptions section.

Since each channel of the 73A-455 must be programmed separately, references to the 73A-455 Module apply to each channel of the module.

- **Order of Commands**

Command order is significant for the 73A-455. The K (preferably) or F command must be the first command issued to the 73A-455 Module after power is applied to the card. Once the F command has been issued, it cannot be reissued unless it is preceded by a K command. After the 73A-455 Module has been programmed to a given mode, other commands can be issued in any order with one exception: a B command must be issued to allocate a buffer before R, S, or D commands can be used to put data into the buffer. New users should follow the order shown in the following mode descriptions until they are thoroughly familiar with the module's operation.

- **Bus Controller Simulator Mode**

Commands available for use in the Bus Controller Simulator mode, in recommended programming order, are:

Command	Description
K	Kill/Reset
H (Optional)	Hi Speed
F	Function
J (Optional)	Jitter
B	Buffer
S	Bus Controller Sequence List
D	Data
M (Optional)	Error Generation mode
V (Optional)	Transmit Voltage Level/Receive Threshold Level
G (Optional)	Gap
T	Trigger
Q (Optional)	Quit
C (Optional)	Condition
A (Optional)	Accept

The first command sent to the 73A-455 following the K command must be an F command to place the module in Bus Controller Simulator mode. After the mode is selected, B commands are issued to allocate buffer space for the Bus Controller Sequence List (see the Glossary for Bus Controller Sequence List definition), and for up to 32 transmit/receive buffers.

Figure 455-3 is a simplified memory map to aid in understanding how the various buffers are set up and interact.

In the Bus Controller Simulator mode, the typical sequence of events that will take place when a T command is received by the 73A-455 Module is as follows (refer to Figure 455-3):

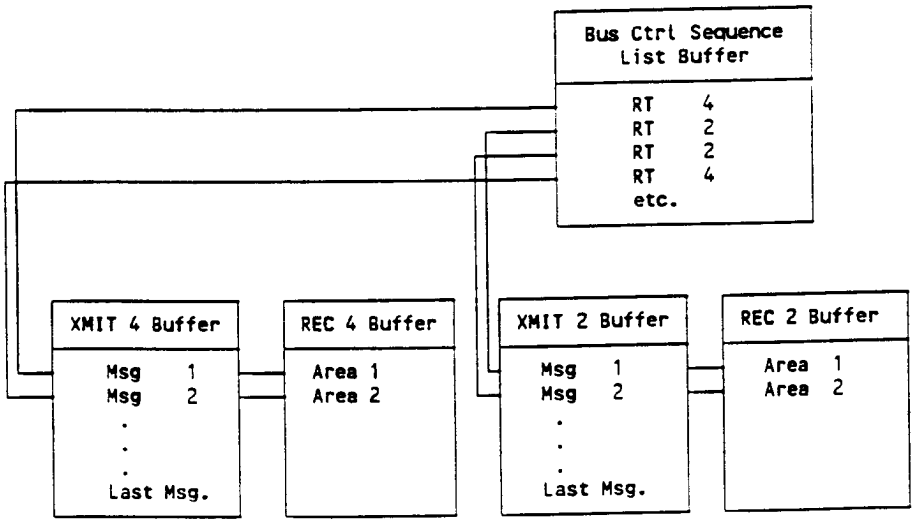


Figure 455-3: Bus Controller Simulator Example

1) The 73A-455 Module will examine the contents of the Bus Controller Sequence List buffer to determine the proper order in which to use the various buffers. The first buffer in the list is buffer 4, so the first message sent will be the first message (Msg 1) contained in transmit buffer 4. Area 1 in receive buffer 4 will receive and store the response to message 1.

   Buffer numbers are usually associated with an RT number. In the Bus Controller mode, however, this is not absolutely necessary.

   Any valid or invalid command word followed by optional data words may be contained in each message. In addition to storing all response, status, and data words received prior to the next command in the receive buffer, the 73A-455 Module also stores the command word in the receive buffer for reference. The command word is stored before the response words. (In the case of an RT-RT command, only the first command word is stored).

2) After the transaction for buffer 4 is completed, the 73A-455 Module takes the next item in the Bus Controller Sequence List. In the example in Figure 455-3, this would be buffer 2. The sequence of events described in Step 1 is repeated, and message 1 in transmit buffer 2's transmit buffer is transmitted.

3) The next Bus Controller Sequence List item is buffer 2 a second time. The second message in transmit buffer 2 is then transmitted.

NOTE: Although Figure 455-3 refers to "Area 1" and "Area 2" for the receive buffers, you only need to allocate a total size for each receive buffer. The card will sequentially load consecutive RT responses. That is, message 2 is loaded immediately following message 1, followed by message 3, etc.

4) The next item in the example is buffer 4 again. This instructs the 73A-455 Module to process the next message in transmit buffer 4. Since the last message processed was message 1, message 2 will be the next one handled.

As this example demonstrates, any number of messages can be handled for any number of RTs in any order, limited only by the amount of memory available on the 73A-455 Module.

To use the Bus Controller mode, first determine the number of buffers required and the access order. The following constraints apply:

- The number of words put into the data buffer should exactly equal the number of transmit words allocated by the B command for proper operation.

- Allocation of <u>both</u> a transmit and receive buffer for any RT to be used is required for proper operation.

- The function that the RT is to perform is an important programming consideration, since all 73A-455 Module buffers are "wrap-around" buffers. Attempting to load too much information may cause information at the front of a buffer to be over-written by new information. Normally, the 73A-455 transmit buffers will be relatively large and the receive buffers relatively small if the RT is to receive, and vice versa if the RT is to transmit.

- The command word needs to be accounted for in allocating receive buffer storage.

Allowing for these constraints, determine the size of each buffer, and allocate the desired buffers.

After the sequence list and transmit and receive buffers have been allocated with the B command, use the following steps to load the desired information into each buffer:

1) Use an S command to specify the order in which buffers will be addressed (Bus Controller Sequence List). The S command is also used to specify the interval between the mid-transition of the parity bit in one message and the mid-transition of the sync pattern in the next message (message pacing).

2) The D command is issued next, to load each transmit buffer in the 73A-455 Module with the proper messages to be sent. An RT receive message consists of a receive command word followed by one or more data words, while an RT transmit message consists of only a transmit command word. Command and data words can be loaded into each transmit buffer in any order.

   The D command is also used to specify the type of induced errors, if any, that are to be placed in the data. Errors may be introduced and tracked on a word-by-word basis. (See the section on Error Handling for a more detailed explanation.)

3) The last word of each message placed in a transmit buffer must be marked with a "last-word flag" in order for the 73A-455 to determine the end of the message and to correlate messages in the transmit buffers with entries in the Bus Controller Sequence List (between MSG1 and MSG2, etc. in the above example).

The preceding steps are the minimum that must be done to program one channel of the 73A-455 Module to operate as a bus controller (between MSG1 and MSG2, etc. in the above example).

Other parameters, which are set to default values in normal operation, can also be programmed. For example, the V command may be used to change the output voltage transmission level from the default value (6.38V ptp), or to change the receive voltage threshold from the default value (2.00V ptp). The value against which the RT's response time is checked can be changed from the default value (4 microseconds) using the G command. An alternate set of transmitted data error types can be selected using the M (Error mode) command.

After all the buffers have been allocated, the data loaded, a bus controller sequence established, and the optional parameters (if any) specified, use a T command to initiate the programmed bus communications sequence. Execution can follow one of three courses, as specified by the T command:

1) The programmed bus communications sequence is executed a specified number of times.

2) The 73A-455 Module is placed in an endless loop and the bus communications sequence is continuously executed until the card is halted with a Q command or External Halt Input signal.

3) The bus communications sequence is stepped forward by one or more messages each time a T command is issued.

After a sequence has been executed, you will usually want to examine the results of the run. The A command allows you to

examine a given buffer word by word, looking at values for received data and errors (if any). The C command allows you to quickly test whether any errors exist in a specified buffer, without having to examine the buffer contents word by word.

The RT address is not required to agree with the buffer number in the Bus Controller mode, which allows more flexible use of the buffers. For example, buffers might be assigned to different subaddresses of the same RT and the Bus Controller Sequence List used to specify the order in which commands are sent to subaddresses.

- **Remote Terminal Simulator Mode**

Commands available for use in the RT Simulator mode, in the recommended order for programming, are:

Command	Description
K	Kill/Reset
H (Optional)	Hi Speed
F	Function
J (Optional)	Jitter
B	Buffer
R (Optional)	RT Response Time List
D	Data
M (Optional)	Error Generation mode
P (Optional)	Sync Pattern
V (Optional)	Transmit Voltage Level/Receive Threshold Level
T	Trigger
Q (Optional)	Quit
C (Optional)	Condition
A (Optional)	Accept

The first command sent to the 73A-455 following the K command must be an FR command to place the card in the RT Simulator mode. After the mode selection is made, a B Command is issued to allocate transmit and receive buffer space for each of up to 31 RTs to be simulated. The transmit buffer for each RT is used to store the message (status and data words) that the RT will return to the bus controller, while the receive buffer is used to store messages (command and data words) sent to the RT by the bus controller.

Transmit and receive buffers must be set up for each RT that the 73A-455 Module is to simulate. If the 73A-455 Module receives messages for an RT which has not been defined by a B command, the associated command and data words will be ignored. In the RT Simulator mode, the buffer number must be the same as the RT terminal number in the command word sent by the Bus Controller.

Figure 455-4 is a simplified memory map to aid in understanding the operation of the 73A-455 Module in the following example. The block at the top of the figure defines the order in which the bus controller will send messages to the 73A-455 Module in this example.

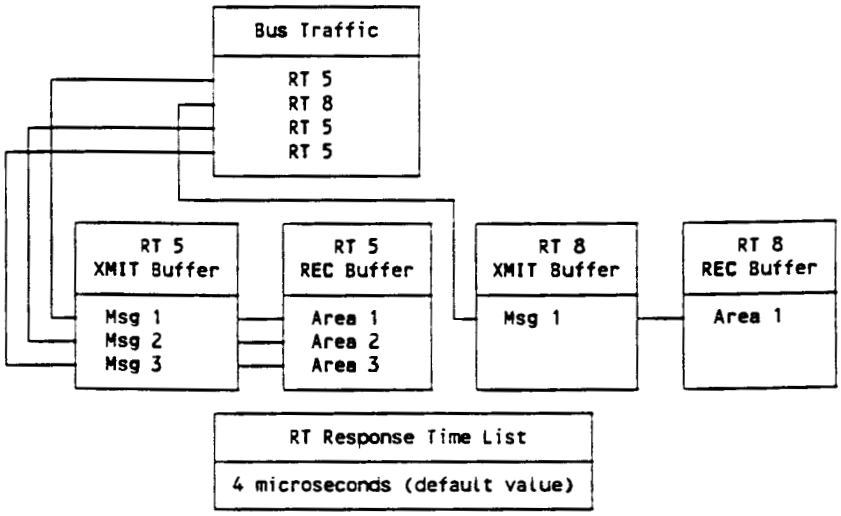


Figure 455-4: RT Simulator Example

Assuming the 73A-455 Module has received a T (Trigger) command, the sequence of events that will take place when the card begins receiving messages from the bus controller is as follows:

1) The first message received by the 73A-455 Module (message 1) is decoded and found to be a transmit command to RT 5. The received message is therefore a single command word, and is stored in RT 5's receive buffer (Area 1 in Figure 455-4).

   Since, in this example, the 73A-455 Module's RT Response Time List was left at its default value of 4 µs for all messages, the 73A-455 Module will transmit the first response message contained in RT 5's transmit buffer with a response time of 4 µs. It is the responsibility of the programmer to load the first response message in RT 5's transmit buffer with a proper status word and the proper number of data words.

2) The next command received instructs the 73A-455 Module to simulate RT 8 in the transmit mode. The received command word will be stored in Area 1 of RT 8's receive buffer. Four µs later, message 1 from RT 8's transmit buffer will be sent to the bus controller. It is the responsibility of the programmer to load the first response message in RT 8's transmit buffer with a proper status word and the proper number of data words.

3) When the third command word is received, a request for RT 5 to transmit again, message 2 in RT 5's transmit buffer is returned to the system controller. The received command word is stored in Area 2 of RT 5's receive buffer.

4) RT 5 is next sent a receive command. The incoming command word and data word(s) will be stored in Area 3 of RT 5's receive buffer. Four µs after the last data word is received, message 3 from RT 5's transmit buffer will be sent to the bus controller. For proper operation, message 3 in buffer 5 must be programmed as a status word and no data words.

Using this pattern, any number of RTs can be simulated to handle any number of messages in any order, limited only by the amount of memory available on the 73A-455 Module.

After the buffers for each simulated RT have been defined with the B command, the next step is to use the D command to load each transmit buffer with the proper status and data words to be returned to the bus controller. The proper status and data words are defined based on the sequence of commands that will be transmitted by the 1553 bus controller. The D command is also used to specify the type of induced errors, if any, that are to be placed in the data. Errors may be introduced and tracked on a word-by-word basis. (See the section on Error Generation for a more detailed explanation.)

These steps represent the minimum setup required to program the 73A-455 Module as an RT simulator. Optional commands are also available which extend the flexibility of the 73A-455 Module by allowing worst-case testing of various 1553 data bus parameters.

In the above example, the 4 µs default RT response time was used when responding to each bus controller command. If desired, a specific RT response time can be associated with each message received by the 73A-455 Module. To do so, a B command is first used to define the size of the RT Response Time List. (The default size is a one-entry list containing a value of four micro-seconds.) The R command is then used to place response time entries in the list.

Each time a message is received, the next available response time from the RT Response Time List will be used to determine the length of time the 73A-455 Module will wait before responding to the received bus controller command. For example, if ten response times were defined, the first response time would be used when processing the first message on the bus, the second response time when processing the second message on the bus, etc. If message 11 was received, the first response time in the RT Response Time List would be used again, since the RT Response Time List is a "wrap-around" list.

Additional optional commands V, P, and M are available in this mode. The V (Voltage) command is used to set the transmit voltage level and receive threshold voltage level, and functions as previously described for the Bus Controller Simulator mode of operation.

The P (Pattern) command instructs the 73A-455 Module not to begin processing messages immediately after receipt of a T (Trigger) command, but rather to wait until a command word is received that contains the 16-bit data pattern defined by the P command. Message processing will begin with the first command word that contains the required pattern. The P command can also be combined with the External Trigger Input to create various types of 73A-455 Module triggering sequences (see the T command in the Detailed Descriptions sub-section).

Transmitted data error types can be selected using the M (Error mode) command.

After all of the buffers have been allocated, the data loaded, and the optional parameters (if any) specified, a T command is issued to initiate the programmed bus communications sequence. Execution can follow one of two courses, as specified by the T command:

1) The number of messages specified by the T command are processed.

2) The 73A-455 Module is placed in an endless loop, and messages are processed until the card is sent a Q command or an External Halt.

NOTE: The 73A-455 Module in the RT mode will remain in a bus active mode until the number of messages as specified by the T command is received. If the messages are not sent, a Q command may be required to terminate the Bus Active mode.

After a sequence has been executed, you will normally want to examine the results. The A command allows you to examine a given buffer word by word, looking at values for received data and errors (if any). The C command allows you to quickly test whether any errors exist in a specified buffer, without having to examine the buffer contents word by word.

- **Bus Monitor Mode**

Commands available for use in the Bus Monitor mode, in the recommended order of programming, are:

Command	Description
K	Kill/Reset
H (Optional)	Hi Speed
F	Function
J (Optional)	Jitter
M (Optional)	Error Generation mode
P (Optional)	Sync Pattern
V (Optional)	Transmit Voltage Level/Receive Threshold Level
T	Trigger
Q	Quit
C (Optional)	Condition
A (Optional)	Accept

As for the other two modes, an F command must be the first command issued following a K command, to place the 73A-455 Module in the Bus Monitor mode. A 30,000-word buffer is automatically allocated. The 30,000-word buffer takes approximately one second to allocate in the hi-speed mode. If several modules are to be chained together as bus monitor modules using the Position Identification Output and External Trigger Input (see Application Note 455-III in Appendix E), they may all be issued an F command prior to data collection to minimize test execution time.

A T command is issued, followed optionally by an F and a number from 1 to 30000, instructing the 73A-455 Module to begin collecting all 1553 bus data.

If an F does not follow the T command, the 30,000-word buffer will function as a wrap-around buffer containing the last 30,000 words received. If an F follows the T command, the 30,000-word buffer will contain the first 30,000 words received. The optional number following the F specifies the position at which the Position Identification Output pulse will be placed on the Position Identification Output line.

A Q command or an External Halt Input signal must be used to stop data collection. The A and C commands have the same meaning and use as described previously for the Bus Controller Simulator and RT Simulator modes (except that only one buffer, rather than 32 buffers, is defined).

The V, P, and M commands, as described for the Remote Terminal mode, are also available in this mode.

- **All-mode Commands**

The following commands are available in every mode:

Command	Description
E	Error - Returns an error code to the system controller which describes any syntax error detected during programming.
H	Hi-Speed - Enables optimized versions of the D (Data), T (Trigger) and A (Accept) commands which significantly improves the execution time of each of those commands. The time required to initialize memory in the monitor mode with the FM command is also reduced significantly.
I	Interrupt - Indicates to the 73A-455 Module if an interrupt is to be sent to the system controller upon completion of a sequence of 1553 bus transactions.
J	Jitter - Enables or disables the detection of transition time errors in the 73A-455 receiver circuitry.
K	Kill - Resets card to power-up state with all parameters set to defaults.

ERRORS

The 73A-455 Module allows several types of errors to be generated to provide for worst-case testing of 1553 bus devices. In addition, errors associated with the 1553 bus can be detected, classified, and stored.

- **Error Generation**

Two different modes of error generation are provided by the M command. Error generation in each mode occurs on an individual word basis. The following types of errors can be generated in the primary error mode:

Sync Error Early - The sync pattern mid-transition will occur one-half bit-time or 500 nanoseconds before the time required by MIL-STD- 1553.

Sync Error Late - The sync pattern mid-transition will occur one-half bit-time or 500 nanoseconds after the time required by MIL-STD-1553.

Incorrect Parity - Even parity will be generated rather than odd parity as specified in MIL-STD-1553.

Manchester error - Manchester encoding specifies that the polarity of the data during the first half of a bit-time shall be opposite the polarity of the data during the last half of the bit-time.

When a Manchester error is specified, the data will be either high or low for the full bit-time depending on whether the data bit is a 1 or 0. The bit position of the error is controlled by the value of the last 4 bits of the word. A hexadecimal value of E through 0 in these 4 bits will generate the error in the first through fifteenth data bits respectively. A hexadecimal value of F will generate the error at the last bit-time prior to the parity bit.

17-bit Word - An additional bit will be added to the transmission prior to the parity bit for a total word time of 21 bits, including sync and parity.

15-bit Word - The last specified bit prior to the parity bit will be omitted from the transmission for a total word time of 19 bits, including sync and parity.

Dropped Bit - Whenever the 1553 bus is active, it is at either a high or low state. If a dropped bit is specified, the bus will go to zero volts for one bit-time at a time other than the 3 sync bit-times or the parity bit-time. The total duration of the word will remain 20 bit-times. The position in the word where the error is generated is controlled in the same manner as that described above for a Manchester error.

An alternate error mode is provided primarily to allow testing a bus controller's or RT's ability to handle bit transitions of ±150 nanoseconds in received data without degradation of receiver performance. The additional error types that can be generated in the alternate error mode are:

Early Sync Transition Time - The sync pattern mid-transition will occur 150 nanoseconds before the time specified by MIL-STD-1553.

Late Sync Transition Time - The sync pattern mid-transition will occur 150 nanoseconds after the time required by MIL-STD-1553.

Dropped Parity Bit - Whenever the 1553 bus is active, it is at either a high or low state. A Dropped Parity Bit will generate zero volts for the parity bit-time. The total duration of the word will remain 20 bit-times,

although if the word is the last word in a message, it will be indistinguishable from a 19-bit word duration.

Single-bit Interword Message Gap - A gap of one μs between two otherwise valid words in a supposedly contiguous message is generated. The gap follows the word for which the error is specified.

14-bit Word/Single-bit Interword Message Gap - This error will generate a word of 2 μs less than normal duration followed by a gap of 1 μs.

Early Bit Transition Time - For one bit-time other than the three sync bit-times or the parity bit-time, the mid-bit transition will occur 150 nano-seconds early. The position in the word where the error is generated is controlled in the same manner as that described previously for a Manchester error.

Late Bit Transition Time - For one bit-time other than the three sync bit-times or the parity bit time, the mid-bit transition will occur 150 nanoseconds late. The position in the word where the error is generated is controlled in the same manner as that described previously for a Manchester error.

Only one type of error may be specified for a particular word; however, each word may have a different type of error, as allowed by the programmed error mode, or no error.

Additional message-formatting errors may be generated as follows:

Incorrect Sync errors may be generated by specifying a data sync for a command or status word, or a command sync for a data word in the data list.

Word Count errors may be generated in the Bus Controller Simulator mode by making the number of data words following the command word different from the word count specified in the command word. Similarly, word count errors may be generated in the RT Simulator mode by making the number of words following the status words different from that specified by the incoming command word.

Interword Message Gaps of 14 μs or more may be generated by specifying an end-of-message flag in the middle of a message. In the Bus Controller Simulator mode, the RT for which the error is generated is entered twice in the Bus Controller Sequence List.

An Incorrect RT Address in a status word is generated by specifying an RT address for the status word different than the RT transmit buffer where the status word is contained.

No RT Response may be generated in the RT Simulator mode by programming the response time to an excessive value so that the response is to the following message on the bus. One entry in the RT Response Time List must be deleted, corresponding to the missing response.

The Transmit/Receive Bit may be made incompatible with the direction of data flow. In the Bus Controller Simulator mode, this is accomplished by setting the T/R bit to RT transmit, then sending data words following the command word, or by clearing the T/R bit to indicate RT receive, and then failing to send data word(s) following the command word.

In the RT Simulator mode, transmit/receive bit incompatibility is accomplished by having only a status word prior to the end-of-message flag when the RT is expecting a request to transmit data,

or sending data words in addition to the status word when the RT is expecting to receive data.

An error which causes more than 32 words of data to be transmitted, in either the Bus Controller Simulator or RT Simulator mode, can be generated by placing the end-of-message flag in a transmit buffer after more than 32 words.

A Response Time error can be generated by programming an excessive response time (up to 65,535 µs) with the R Command.

Any other errors which are dependent on the command or status word contents or the number of words transmitted may be simulated by defining those invalid words or messages in the transmit buffers. They include improper mode code usage, invalid subaddresses, illegal commands, and improper use of the status word bits.

- **Error Detection**

The error types detected by the 73A-455, their decimal assignment (value of second byte in response to the A command), and definitions are:

Excessive Gap Time (1)

If an RT does not respond to a controller command from the 73A-455 Module within the time specified by the G (Gap) command, an Excessive Gap Time error will be recorded. This error is recorded for each word of the RT's response message unless an error of higher priority is detected.

Parity error (2)

If even parity is detected in an otherwise acceptable 20-bit word, a Parity error will be recorded.

Manchester error (3)

An invalid Manchester pattern (signal during the last half of a bit-time is not opposite the level during the first half of the bit-time) that is also not a valid sync pattern (to distinguish this error from a Too Few Bits error) will be recorded as a Manchester error.

Sync error (4)

When an invalid sync pattern that is also not a valid Manchester pattern (to distinguish this error from a Too Many Bits error) occurs at the time when a sync pattern is expected (at the beginning of a transmission or 20 bit-times after the start of the last valid sync pattern), then a Sync error will be recorded. At the beginning of a transmission, the width of the 1.5 µs first half of the sync pulse is also tested. The width must be from 1.4 to 1.72 µs.

Too Many Bits (5)

Lack of a valid sync pattern or gap (zero level on the bus) within 20 bit-times after the last valid sync pattern will be recorded as a Too Many Bits error. This error will actually be reported on the word following the word in error. When a Single Error bit is detected on the last word of a message, an error may not be reported, since this condition is indistinguishable from permissible noise during transmitter shutdown. When several extra bits are detected on the last word of a message, they will be treated as an additional data word, typically a word with too few bits.

Too Few Bits (6)

A valid sync pattern that occurs less than 20 bit-times following the last valid sync pattern, or a gap (zero level on the bus) that occurs and doesn't recover within 20 bit-times (to distinguish it from a Dropped Bit error) after the last valid sync

pattern, will be recorded as a Too Few Bits error.

This error will actually be reported on the word following the word in error unless the condition occurs on the last word of a message, in which case the error is reported on the failing word. In addition, if the error occurs in other than the last word in a message, the sync pattern of the following word will cause a Manchester error to be recorded on the failing word.

Dropped Bit (7)

A gap (zero level on the bus) of one or more bit-times that recovers within 20 bit-times after the start of the last valid sync pattern will be recorded as a Dropped Bit error. The dropped-bit-error latch will not be cleared until the start of the next message and Dropped Bit errors will be recorded on all words remaining in the present message.

Incorrect Bit Transition Time (8)

All 0-to-1 and 1-to-0 transitions of the bus are checked to see whether they are within 62.5 to 125 nanoseconds of the expected transition time. The acceptance window is 187.5 nanoseconds wide, and slides from 62.5 to 125 nanoseconds on either side of the expected transition time, depending on the phase relationship between the incoming signal and the internal 73A-455 Module 16 MHz clock.

Once an Incorrect Bit Transition Time error occurs in a message, data may not be recorded correctly until the start of the next message, and the error will be recorded for all words until the end of the message. This error detection may be inhibited with the J command. Crossing times are measured at the receiver threshold point (1.0 and -1.0 volts for a 2.0 V ptp receive threshold setting, for example).

Although this is a useful "quality of signal" test when the 73A-455 is closely attached to a unit under test, the error may need to be ignored under actual bus operational conditions (due to bus noise or transmission reflection problems).

Word Count error (9)

In the Bus Controller Simulator mode, a Word Count error will be recorded if an RT does not respond with the number of words requested by the command word.

In the Bus Monitor mode, a word count error will be reported if either the bus controller command or the remote terminal response does not contain the proper number of words. In the RT Simulator mode, a Word Count error will be recorded if the bus controller under test sends a command word that is not consistent with the transmit/receive bit and number of words specified in that command word. A Word Count error will be reported only on the first word of a message.

Message Format error (10)

The message received was not a valid 1553 format for the particular mode selected. The error must be caused by something other than a wrong number of data words. A Message Format error will be reported on each word of the message in error. The error may, of course, be overridden by a higher priority error, on a word-by-word basis. Message format error detection is described in more detail in the Command Checking section.

No Data error (11)

No data has been loaded into the receive buffer.

Interword Gap error (12)

A word is followed by an unexpected gap, or a word is not followed by an expected gap. This error is distinguished from a "word count" error in that the proper number of data words occurred between two command words; but a gap occurred at other than the end of the message, or no gap occurred between messages. The error is reported on a word-by-word basis.

Only one of the above errors will be recorded for a particular word. If more than one error exists in a word, error logging will proceed according to the following priorities:

Highest	-	error type 8
Next highest	-	error type 7
Next highest	-	error type 6, 5
Next highest	-	error type 4
Next highest	-	error type 3
Next highest	-	error type 2
Next highest	-	error type 1
Next highest	-	error type 9
Next highest	-	error type 10
Lowest	-	error type 12

Error types 9, 10, and 12 are reported only when using the formatted hexadecimal format (HF) when accepting data with the A (Accept) command.

In MIL-STD-1553A applications where mode codes and status word bits are less well defined, the HF format should not be used.

A decimal value 11 in the error code field indicates that no more data is available. This does not indicate an error.

- **Command Checking**

This section describes in detail the Message Format errors (error type 10) detected by the 73A-455.

Mode code commands are checked for proper presence or absence of a data word and direction of the data word (depending on the mode code), and also for proper use of the broadcast command.

Broadcast commands are checked for absence of a response.

RT-to-RT commands are checked for response by both RT's, consistent RT numbers, proper use of the T/R bit, word count in both command words, and consistent actual word count.

RT-to-RT broadcast commands are checked for no response by a receive RT.

Illegal use of mode codes in an RT-to-RT transfer is checked.

The contents of the status word in both normal and RT-to-RT transfers are checked for the following:

- Reserved bits should not be set.
- The instrumentation bit should not be set in a status word.
- The busy bit should be accompanied by no data words even if data words are requested.
- A message error bit will be marked as a message format error.
- Broadcast received bit and dynamic bus controller acceptance bits are checked to see that they only occur in response to a transmit status mode command.

The C (Condition) command also checks for the above format errors.

NOTE: Proper use of format checking requires that the receive buffer not have been wrapped. The C command also requires that the data be followed by at least one No Data Word indication.

NOTE: Checking of RT-to-RT format errors in the RT Simulator mode is limited. The use of the RT Simulator in RT-to-RT transfer must be restricted to well-defined situations and is discussed further in the Application Note on RT-to-RT Transfers in Appendix D.

COMMAND DESCRIPTIONS

- **Command Syntax**

Command protocol and syntax for the 73A-455 Module are as follows:

- Each command consists of a single line of up to 240 characters. Parameters may not be "wrapped around" (continued on the next line). Every command must end with a carriage-return <CR>. Line-feeds <LF> are optional. In some cases a line feed may significantly slow down an operation.

- If a given parameter is to be skipped, left at its previous value, or have its default value accepted, its position must still be denoted using consecutive commas.

- If a character is not enclosed by brackets, that character itself is sent, otherwise:

[]	encloses the symbol for the actual argument to be sent. These argument symbols are defined under each command heading.
<CR>	indicates a carriage-return.
<LF>	indicates a line-feed.

- All characters must be sent in upper case form.

This module does not accept superfluous spaces. Some controllers automatically add spaces to fill the command string. If your controller adds these spaces, see your controller manual to determine how to suppress the spaces. The HP-85 and HP-86 controllers, for example, require using a "K"; command argument to suppress spaces.

In the command descriptions, MSB indicates the Most Significant Bit, and LSB indicates the Least Significant Bit.

- **Detailed Descriptions**

A detailed description of each command, in alphabetical order, is given on the following pages.

Command: A (Accept)

Syntax: Az_1,z_2,z_3

Purpose: The A (Accept) command specifies the data which the 73A-455 Module is to pass back to the system controller in response to the next system controller input request, and the format for this data. This is a required command.

Description: This description contains the definition of the z_1,z_2,z_3 parameters, the syntax of the returned data for each format, how to use the A command, a tutorial, and examples.

In the Bus Controller Simulator mode or RT Simulator mode, z_1 specifies the number of the receive buffer (0-31) from which the data and error information are to be collected. In the Bus Monitor mode, z_1 must be an asterisk (*, Octal 52), indicating the single large receive buffer allocated in the Bus Monitor Mode.

z_2 is a number from 1 to 30000 that specifies the location within the selected receive buffer for the start of data and error collection. Data will be read back starting at that location in the buffer.

z_3 is one of the following ASCII characters, which specifies the format of the returned data:

H Hexadecimal - only word level checking.
HF Hexadecimal with Message Format Checking - word level checking, checks for word count and message format errors.
HE Hexadecimal with Extended Message Format Checking - word level checking, checks for word count and message format errors, identifies command versus status words, and indicates whether a gap in data bus activity follows the word.
B Binary
BL Blocked Binary

z_3	Controller receives:
H, HF, or HE	six hexadecimal characters, followed by <CR> and <LF> for each input request.
B	three 8-bit binary bytes followed by <CR> and <LF> characters.
BL	three 8-bit binary bytes with no <CR> or <LF> until a No-Data word is detected. The No-Data word three bytes

will then be followed by <CR> and <LF> characters. If a No-Data word is not detected (the receive buffer has wrapped), the system controller may terminate input in the Blocked Binary mode at any time by issuing a new output command to the card.

After the Accept command is issued, the system controller normally begins requesting input from the 73A-455 Module. The complete syntax of the returned data for each format is as follows:

H and HF Format: (6 hex characters)

1st character -

0 indicates a data word.
1 indicates a status or command word.

2nd character - Error Code/No Data

Value	Error
0	No Errors
1	Excessive Response Time
2	Incorrect Parity
3	Manchester Error
4	Sync Error
5	Too Many Bits
6	Too Few Bits
7	Dropped Bit Error
8	Bit Transition Time Error
9	Word Count Error*
A	Message Format Error*
B	No Additional Data
C	Interword Gap Error*

* Available only when z_3 is specified as HF or HE

For a complete description of error types, see the Error Handling subsection.

3rd through 6th characters -

Hexadecimal equivalent of the 16 data bits in the command, status, or data word. The MSB of byte 3 is the first data bit transmitted on the bus. The LSB of byte 6 is the last data bit transmitted on the data bus.

7th character - Carriage-return <CR>.

8th character - Line-feed <LF>.

HE Format: (6 hex characters)

The data is formatted the same as the HF format for characters 3 through 8. For the HE format, the first and second characters are redefined as follows:

1st character -

Value	Word Type	Gap Following
0	Data Word	No
1	Command Word	No
2	RT-RT Transmit Command	No
3	Status Word	No
4	Data Word	Yes
5	Command Word	Yes
6	RT-RT Transmit Command	Yes
7	Status Word	Yes

2nd character -

Codes 0 through C are the same as the HF format. An additional code D has been added for the HE format, which indicates that no data was received because the Trigger command to the module was aborted by a Q (Quit), K (Kill) or external Halt input before the trigger actually occurred.

B and BL Format: (3 8-bit binary bytes)

1st Byte -

The three most significant bits are set to 0. The next bit is 0 if the word is a data word and 1 if the word is a status or command word. The four least significant bits contain the error code, defined as follows:

Low Order Four Bits	Error/No Data
0000	No Errors
0001	Excessive Response Time
0010	Incorrect Parity
0011	Manchester Error
0100	Sync Error
0101	Too Many Bits
0110	Too Few Bits
0111	Dropped Bit Error
1000	Bit Transition Time Error
1011	No Additional Data

For a complete description of error types, see the Error Handling subsection.

2nd and 3rd Bytes -

These bytes contain the 16 data bits of the command, status, or data word. The MSB of the second byte is the MSB of the 16-bit data word

and the first data bit transmitted on the bus. The LSB of the third byte is the LSB of the 16-bit data word and the last data bit transmitted on the bus.

Using the Accept Command

The Accept command is a required command. If an Accept command, Condition command, Error command, or TEST command is not sent before requesting a response from the 73A-455, a ?<CR><LF> will be returned in response to an Input Request.

When the A command is used to return binary or hexadecimal data to the system controller, keep in mind that each data buffer is a wrap-around buffer. The 73A-455 Module will continue sending data to the system controller from the specified buffer until the system controller stops requesting input.

For example, if a given buffer is 50 words long, and the system controller requests 100 words, the buffer will be transmitted twice. If each buffer is specified to be slightly larger than the expected amount of data to be received into the buffer, then the No Additional Data code can be used by the system controller to determine when to stop requesting input from the 73A-455 Module.

In the Blocked Binary Accept command format, the No Additional Data code is used to append a <CR> and <LF>. In IEEE-488 systems, the <LF> may be used to generate an EOI and automatically terminate input following the first No Data word.

Tutorial: Derivation of MIL-STD-1553B Command Word Content From Hexadecimal Data

MIL-STD-1553B requires a specific format for the bus controller command word. The first five bits transmitted are the RT Terminal Address, the sixth bit is the Transmit/Receive bit, the next five are the RT sub-address, and the last five bits are the word count. As an example, the command word content of "D423h" would be derived as follows:

1. Write down the bit pattern corresponding to the hexadecimal value, D423: 1101 0100 0010 0011

2. Reblock the bits in groups of 5, 1, 5 and 5 bits to correspond to the command word format: 11010 1 00001 00011

3. Determine the decimal value of each block. For example, 11010 equals decimal 26.

The resulting command word contents for this example are:

RT Address	26
T/R bit	Set
Sub-address	1
Word Count	3

Example: To obtain data beginning at the start of the buffer associated with RT 26, using hexadecimal data format, the following Accept command would be issued: A26,1,H

If buffer 26 contained a status word and three data words, with the second data word containing an incorrect parity bit, the following might be returned to the system controller if input was requested five times from the 73A-455 Module:

Input	Data Returned:	
Request	H, HF, HE Format	B Format
1st Byte	2nd Byte	3rd Byte
1st	10D100 <CR><LF>	<00010000><11010001><00000000><CR><LF>
2nd	00B6AD <CR><LF>	<00000000><10110110><10101101><CR><LF>
3rd	02B6AF <CR><LF>	<00000010><10110110><10101111><CR><LF>
4th	0008F6 <CR><LF>	<00000000><00001000><11110110><CR><LF>
5th	0B0000 <CR><LF>	<00001011><00000000><00000000><CR><LF>

Command: B (Buffer)

Syntax: Bz_1,z_2

Purpose: The B (Buffer) command is used to allocate 73A-455 Module buffers.

Description: The Buffer command allocates the size of the 32 transmit and receive buffers in the Bus Controller and Remote Terminal modes. It also allocates the size of the Sequence List buffer in the Bus Controller mode and the Response Time List buffer in the Remote Terminal mode. The Buffer command is a required command.

Misuse of the Buffer command is the most common cause of improper operation in new applications. Careful attention to the Buffer Specification Rules on the required parameters for the Bus Controller and Remote Terminal modes on the next page will help minimize problems in using this command.

Bus Controller Simulator Mode:

In the Bus Controller Simulator Mode, the B command is used to allocate the 32 transmit and receive buffers as well as a buffer for the Bus Controller Sequence List.

Transmit buffer

z_1 the buffer number (0 to 31). Setting z_1 to an "*" (Octal 52) will size all 32 buffers to the same size.

z_2 a T followed by the decimal size of the buffer.

Receive buffer

z_1 the buffer number (0 to 31). Setting z_1 to an "*" (Octal 52) will size all 32 buffers to the same size.

z_2 an R followed by the decimal size of the buffer.

Bus Controller Sequence List buffer

z_1 an S followed by the decimal size of the Bus Controller Sequence List.

z_2 not used.

Transmit and receive buffer numbers are very often associated with RTs of the same number. However, in the Bus Controller Simulator mode, this is not absolutely necessary. In this mode, buffers may also be used for subaddresses, or to agree with the sequence of messages (buffer 0 for the first message, buffer 1 for 2nd message, etc.), for example.

RT Simulator Mode:

In the RT Simulator Mode, the B command is used to size the receive and transmit buffers for each simulated RT and the optional RT Response Time List buffer, if required.

Transmit buffer

z_1 the RT number (0 to 31). Setting z_1 to an "*" (Octal 52) will size all 32 buffers to the same size.

z_2 a T followed by the decimal size of the buffer.

Receive buffer

z_1 the RT number (0 to 31). Setting z_1 to an "*" (Octal 52) will size all 32 buffers to the same size.

z_2 an R followed by the decimal size of the buffer.

RT Response Time List buffer

z_1 an R followed by the decimal buffer size.

z_2 not used.

In the RT Simulator Mode, the 73A-455 Module detects the RT address of an incoming command word and uses that to select the buffer number to respond from. The buffer number therefore must be associated with an RT (buffer 8 used to respond to RT 8 command words, etc.) in the RT Simulator Mode. An incorrect RT address in a status word may be simulated, however. The buffer number only has to agree with the RT address of the incoming command word. The status word RT address may be different than the buffer number.

Bus Monitor Mode:

The B command is not required in the Bus Monitor Mode. In the Bus Monitor Mode, a single 30,000 word receive buffer is automatically allocated by the 73A-455 Module.

Buffer Specification Rules:

The buffers allocated by the B command are wrap-around buffers, so if additional data are written into a full buffer, the additional data will be stored starting back at the first location in the buffer.

If the sequence list is to execute more than once, or if a transmit buffer is to be transmitted more than once, it must be allocated exactly equal to the number of words to be loaded by the commands that define the contents of the buffer (the Sequence or Data commands). Otherwise, improper

transmission will result. The 73A-455 Module, when triggered, will transmit any undefined data when it reaches the end of the defined data. Only when it reaches the end of the buffer will it return to the top of the buffer.

Transmit and receive buffers must be allocated in pairs. Improper operation will result if a transmit buffer is allocated for a given buffer without also allocating a receive buffer. If received data is not of interest, then a one-word receive buffer may be allocated and the data ignored.

In the Bus Controller mode, the bus controller command word is stored in the receive buffer for easy correlation of command and response. So, when sizing the receive buffer, allow one additional location for each command/response.

Examples:

Bus Controller Simulator Mode:

To set up a Bus Controller Sequence List with space for one entry, a transmit buffer of one word for buffer 17, and a receive buffer of 34 words for buffer 17, the following three commands would be issued:

```
BS1
B17,T1
B17,R34
```

These allocations would be appropriate for a 32 data word transmit message to Remote Terminal 17, for example. The 34 word receive buffer allows storage of the command word (which is stored in the receive buffer on transmission), the returned status word, and 32 data words.

RT Simulator Mode:

To set up transmit buffers of 33 words each and receive buffers of two words each for RTs 23 and 9 (representing, for example, one status word and 32 data words in the transmit buffer, and one command word followed by a No Data word in the receive buffer), the following four commands would be issued:

```
B23,T33
B23,R2
B9,T33
B9,R2
```

In this example, it is assumed that the default RT Response Time List of a single word is acceptable. If a different response time is desired for RT9 and RT 23, use the command BR2 to allocate an RT Response Time List of 2 words.

Command: C (Condition)

Syntax: Cz

Purpose: The C (Condition) command is used to examine all data stored in the 73A-455 Module memory for a given RT buffer, on a block-by-block basis, to determine if any message block contains an error.

Description: z is a decimal number (0 to 31) which specifies the buffer for which a condition check is to be made. In the Bus Monitor mode, the z parameter is ignored and may be omitted.

After issuing the C command, the system controller will request input from the 73A-455, and receive a response consisting of a single digit (0, 1, or 2) followed by a <CR> and <LF>. The response digit indicates the state of the receive buffer for the specified RT:

0 Indicates that the buffer contains no data words with errors.

1 Indicates that the buffer contains at least one word containing one of the following errors:

- Too few bits
- Incorrect parity
- Too many bits
- Excessive response time
- Sync error
- Manchester error
- Dropped bit error
- Bit transition time error
- Word count error
- Message format error
- Interword gap error

2 Indicates that condition checking is not possible because the number of words received exceeded the size of the specified buffer, causing the 73A-455 Module to wrap memory and overwrite messages at the beginning of the buffer, or that the received data exactly filled the buffer and the 73A-455 Module was unable to positively indicate that the data was valid. To use the C command, receive buffers should be sized to allow at least one No Additional Data word at the end of a buffer.

Normally, the C command will be used when the 73A-455 Module is programmed to process a finite number of messages. It indicates to the system controller whether or not it is necessary to issue an A command and examine each word in the receive buffer.

See the Error Detection subsection for a complete description of what the detected errors mean, including a discussion of the types of errors included as message format errors.

Command: D (Data)

Syntax: $Dz_1,z_2,z_3,z_4,...$

Purpose: The D (Data) command specifies the data list for any one of the 32 transmit buffers in the Bus Controller or Remote Terminal modes.

Description: z_1 specifies the number (0 to 31) of the buffer to which the data list applies.

z_2 is a number in the range of 1 to 30000 that specifies the starting buffer position for the data list. The z_2 value is provided to allow definition or update of data values in the buffer without having to start at the top of the buffer.

z_3 is either H (Hexadecimal) or B (Binary), specifying the format for the data.

z_4 is the actual data list.

In Bus Controller Simulator mode, the D command loads into memory the command and data words to be sent from the specified buffer.

In RT simulator mode, the D command loads into memory the status and data words that a specific RT will send to the bus controller in response to a command word with an RT address equal to the RT buffer number as specified by z_1.

The D command allows an end-of-message flag to be programmed and can therefore be used to program multiple messages in a buffer.

Hexadecimal Format:

If z_3 is an H, then the format of z_4 is groups of six ASCII characters as defined below. Each six character value is separated by commas, and each message is separated or terminated with a semicolon. Examples are given below.

1st Character -

0 Indicates a data word.

1 Indicates a command or status word.

2 Indicates a data word to be followed by a low TTL pulse on the Position Identification Output. The TTL pulse occurs during the sync pattern of the following word.

3 Indicates a command or status word to be followed by a low TTL pulse on the Position Identification Output. The TTL pulse occurs during the sync pattern of the following word.

If the last word in a message is programmed with a 2 or 3, the Position Identification Output pulse will be generated during the beginning of the next transmitted command word for that RT.

2nd Character - Error code, 0 through 7.

For primary error mode (no M command, or M0 command programmed):

Value	Error
0	No errors
1	Sync transition 500 ns early
2	Incorrect parity
3	Manchester error
4	Sync transition 500 ns late
5	17-bit word
6	15-bit word
7	Dropped bit

If the alternate error mode has been programmed (M1 command):

Value	Error
0	No errors
1	Mid-sync transition 150 ns early
2	Dropped parity bit
3	Mid-bit transition 150 ns late
4	Mid-sync transition 150 ns late
5	1-μs gap following word
6	14-bit word followed by 1-μs gap
7	Mid-bit transition 150 ns early

3rd through 6th Characters -
The 16-bit command, status, or data word, which is represented by four hexadecimal digits. The MSB of the first hexadecimal digit is the first bit transmitted on the MIL-STD-1553 bus following the sync pattern. The LSB of the fourth hexadecimal digit is the last bit of the 16-bit word transmitted before the parity bit.

The delimiters following z_4 must be commas (,) unless z_4 is the last word of a message. If z_4 is the last word of a message, then a semicolon (;) must be used. This convention must be followed even if z_4 is the last word of a line of data. Remember that a line of data is restricted to a maximum of 240 characters.

A colon rather than a semicolon may be used to separate messages and end the last message. Leading zeros are assumed if less than six hexadecimal digits are specified.

Binary Format:

If z_3 is a B, then each command, sync, or data word consists of three 8-bit bytes.

The first byte is formatted as follows:

8th Bit (MSB) — Set to 1 if this is the last word to be loaded by this D command; allows <CR> or <LF> characters to be sent again to the 73A-455 Module.

7th Bit — Set to 1 if this word is to be followed by a low TTL pulse at the Position Identification Output; set to 0 otherwise.

6th Bit — Set to 1 if this is the last word of a 1553 bus message.

5th Bit — Set to 1 if this is a command or status word; set to 0 if this is a data word.

4th through 1st Bits — The low order four bits are used to contain the error code:

For primary error mode (no M command, or M0 command programmed):

Low Order Four Bits	Error
0000	No errors
0001	Sync transition 500 ns early
0010	Incorrect parity
0011	Manchester error
0100	Sync transition 500 ns late
0101	17-bit word
0110	15-bit word
0111	Dropped-bit error

For alternate error mode (M1 command programmed):

Low Order Four Bits	Error
0000	No errors
0001	Mid-sync transition 150 ns early
0010	Dropped parity bit
0011	Mid-bit transition 150 ns late
0100	Mid-sync transition 150 ns late
0101	1 µs gap following word
0110	14-bit word followed by 1 µs gap
0111	Mid-bit transition 150 ns early

The second and third bytes contain the 1553 bus data word. The MSB of the second byte is the first bit of the 16-bit word transmitted following the sync

pattern. The LSB of the third byte is the last bit of the 16-bit word transmitted prior to the parity bit.

In the binary format, the restriction of 240 characters per line does not apply. A line may be of any length. If desired, the binary transfer can be separated into smaller transfers by using bit 7 of byte 1 to indicate the end of the transfer, and z_2 of the D command to position the start of the next transfer.

Examples: Example 1:

If the 73A-455 Module is functioning as a bus controller simulator, and you wish to load the command word and three data words shown below into transmit buffer 26 (used for RT 26 in this example), beginning at buffer position 1, use the following D command:

Hexadecimal Format:
D26,1,H,10D023,05B6AD,00B6AF,0008F6;

Type Word	Binary Data MSB LSB	Hex. Data	Errors
CMD	1101000000100011	D023	None
DATA	1011011010101101	B6AD	17-bit word
DATA	1011011010101111	B6AF	None
DATA	0000100011110110	08F6	None

To load the same data to RT 26 using binary format, use the following D command:

Binary Format: D26,1,B,d1d2d3d4...d12

Where d1 through d12 represent 12 8-bit bytes (3 8-bit bytes for each of 4 words) sent to the 73A-455 Module. The binary values of the bytes d1 through d12 are shown below:

Byte	Value	Notes
1	00010000	Cmd Word
2	11010000	D0
3	00100011	23
4	00000101	Data w/err 5
5	10110110	B6
6	10101101	AD
7	00000000	Data/No Errors
8	10110110	B6
9	10101111	AF
10	10100000	Data/End of Msg/Last 3 Bytes
11	00001000	08
12	11110110	F6

In the BASIC programming language, binary data is often transmitted by using the CHR$ function to build a string. A string WRT$, for the example above, would be created as follows:

WRT$ = "D26,1,B," + CHR$(16) + CHR$(208) + CHR$(35) + CHR$(5) + CHR$(182) + CHR$(173) + CHR$(0) + (CHR$(182) + CHR$(175) + CHR$(160) + CHR$(8) + CHR$(246)

Note that byte 10 above has bit 8 and bit 6 both set to indicate end of message and also to indicate the end of the binary transfer.

Example 2:

This example illustrates how to derive a four character hexadecimal command word for a desired command per MIL-STD-1553. Assume an RT address of 27, the T/R bit set, a subaddress of 1, and a word count of 17. The 16 bit pattern required for this command word is as follows:

RT 27	T/R Bit Set	Subaddr 1	Word Count 17
11011	1	00001	10001

Combine the bits and separate into groups of four as follows:

1101 1100 0011 0001

The resulting four hexadecimal characters are DC31.

Command: E (Error)

Syntax: E

Purpose: When the 73A-455 Module receives a command from the system controller that it is unable to recognize, the ERR LED on the front edge of the module is lit. Use the E command to determine the type of error that caused the ERR LED to light.

Description: The E command instructs the 73A-455 Module to return the appropriate two-digit syntax error code as a response to the next input request to the 73A-455 Module.

The possible error codes are:

Value	Error
00	No error
01	Unrecognizable command
02	Command line too long
03	Memory full
04	Invalid A (Accept) command
05	Invalid B (Buffer) command
06	Invalid C (Condition) command
07	Invalid D (Data) command
08	Invalid E (Error) command
09	Invalid F (Function) command
10	Invalid G (Gap) command
11	Invalid I (Interrupt) command
12	Invalid M (Error Mode) command
13	Invalid P (Pattern) command
14	Invalid Q (Quit) command
15	Invalid R (Response Time) command
16	Invalid S (Sequence) command
17	Invalid T (Trigger) command
18	Invalid V (Voltage) command
19	Invalid input request

When the error code is returned following the E command, the error code is cleared and the ERR LED is turned off.

In an ATE system, it may be useful to determine if a syntax error has occurred, especially during program development. The E command may be sent after each command to determine if the command caused a programming error. If no error has occurred, then error code 00 will be returned, indicating no syntax error.

If an E, A, C, or TEST command is not sent before requesting a response from the 73A-455, a ?<CR><LF> will be returned in response to an input request to the module.

Command: F (Function)

Syntax: Fz

Purpose: The F (Function) command selects the 73A-455 Module's function: bus controller simulator, RT simulator, or bus monitor.

Description: z is one of the following:

C - Bus Controller Simulator
R - RT Simulator
M - Bus Monitor

The K (preferable) or F command must be the first command issued to the 73A-455 Module after power is applied to the card. After the F command has been issued, the F command cannot be reissued unless it is preceded by a K command.

An FM command requires approximately 1 second to allocate a 30,000-word buffer. If multiple cards are to be chained together in the Bus Monitor Mode to achieve continuous collection of more than 30,000 words, the F command should be issued to all cards before sending the T command to the first card in the chain.

If the card is not in the high speed mode (see H command), allocation of the buffer requires approximately 7 seconds.

Example: The command FM will cause the MON LED to light and the 73A-455 Module to function as a bus monitor.

Command: G (Gap)

Syntax: Gz

Purpose: When the 73A-455 Module is functioning as a bus controller simulator, it automatically checks the response time of each RT with which it communicates. The G command specifies the time in microseconds against which each RT's response time will be checked.

Description: z is a 1- or 2-digit decimal number from 4 to 31 that specifies the value of the response time gap in microseconds. (See the Glossary for a definition of RT Response Time.)

If an RT responds, but fails to respond in the time programmed by the G command, the response-time error will be logged along with the first word (status or data) received from the RT. If the RT does not respond at all, there will simply be no data in the respective RT's receive buffer.

If the RT waits to respond until the 73A-455 Module has begun outputting its next message, a "data collision" or "bus crash" will occur on the bus, and data may be garbled. (A "data collision" is defined as two devices attempting to transmit on the 1553 bus at the same time.) If this happens, the offending RT's receive buffer will contain no additional data, since the receive logic on the 73A-455 Module is disabled while the card is transmitting data.

Example: The command sequence G12 would set the response time gap test value to 12 microseconds as specified in MIL-STD-1553B.

Command: H (High Speed)

Syntax: Hz

Purpose: The H (High Speed) command optimizes the execution time of the F (Function), D (Data), T (Trigger), and the A (Accept) commands.

Description: z is a decimal number (0 or 1) which specifies:

0 - Disable high speed operation
1 - Enable high speed operation (default)

On power-up, the high speed mode will be enabled.

The set of commands chosen for optimized performance allows use of the modules in applications where one or two small messages may need to be updated in response to the results of a previous message in a 50 millisecond time frame.

The high speed operation is not intended to accommodate complex Real Time simulation applications. The 53A-454 MIL-STD-1553 Real Time Bus Controller Simulator Card is available for those applications.

During the FM command, the High Speed mode also speeds up the allocation of the 30,000 word receive buffer from 7 to 1 seconds.

Example: The command sequence H1 enables high speed operation.

Command: I (Interrupt)

Syntax: Iz

Purpose: The I (Interrupt) command enables the interrupts from the 73A-455 Module.

Description: z is a decimal number (0 or 1) which specifies:

0 - Disable interrupt generation (default)
1 - Enable interrupt generation

If the interrupt mode is enabled, the 73A-455 Module will generate an interrupt when a 1553 bus communications sequence is completed. The interrupt is cleared when the system controller requests input from the 73A-455 Module.

The interrupt generates a VXIbus interrupt at the level set by the Interrupt Level Select switch (see Switches subsection). In IEEE-488 applications, this interrupt may be used to generate a Service Request (SRQ), assuming the Interrupt Level Select switch on the handler module for the 73A-455 (the 73A-151 Slot 0 Module in the case of a CDS/Tek 73A-IBX System) is set at the same level as the Interrupt Level Select switch on the 73A-455.

Example: The command sequence I1 enables interrupts.

Command: J (Jitter)

Syntax: Jz

Purpose: The J (Jitter) command disables transition time error detection by the receiver of the 73A-455 Module.

Description: z is a decimal number (0 or 1) which specifies:

0 - Enable transition time error detection (default)
1 - Disable transition time error detection

At power-up and following a K (Kill) command the transition time error detection is enabled.

The transition time detection measures the time from one threshold crossing to the next threshold crossing, which is nominally expected to be 0.5, 1.0, 1.5 or 2.0 microseconds, per MIL-STD-1553.

The receiver checks that this time is reliably within 62.5 nanoseconds of the nominally expected time (threshold crossing points are +1.0 V and -1.0 V for rising and falling signals respectively when the receiver threshold is programmed to 2.0 V ptp.).

A receiver transition time error (Error 8) may be generated when the time from one threshold crossing to the next is out of tolerance by more than 62.5 nsec.

Although this is a useful "quality of signal" test when the 73A-455 is closely attached to a unit under test, the error may need to be ignored under actual bus operating conditions, due to transmission reflection problems associated with system level cabling between devices on the bus and the 73A-455 receiver.

Example: Issuing the command sequence J1 will disable the transition time error detection until another K (Kill) command is issued.

Command: K (Kill)

Syntax: K

Purpose: The K command instructs the 73A-455 Module to restore its power-up conditions.

Description: The status of the 73A-455 after a K command is as follows:

Interrupt:	Disabled (I command)
Transmit Level:	6.38V ptp (V command)
Equivalent Bus Load for Transmit Level:	70 ohms (V command)
Receive Threshold:	2.00V ptp (V command)
Response Gap:	4 µs (R command)
Pace Interval:	1,000 µs (S command)
RT Response Time Test Value:	12 µs (G command)
Mode:	Undefined (F command)
Pattern Trigger:	Disabled (P command)
Error Mode:	Primary error set selected (M command)
RT Response Time List:	Unallocated (B command)
RT Sequence List:	Unallocated (B command)
Transmit and Receive Buffers:	Unallocated (B command)
Hi Speed Mode:	Disabled (H command)
Transition Time Error Detection:	Enabled (J command)

Example: Issuing the K command at any time will restore the 73A-455 Module to its initial power-up condition as defined above.

NOTE: The Q and K commands are the only commands that can be issued to the 73A-455 Module while a bus communications sequence is in progress without hanging up the system controller. For a further discussion of how to avoid hanging up the system controller during bus communications sequences, see the note following the T command.

Command: M (Error Mode)

Syntax: Mz

Purpose: The M (Error Mode) command selects one of two different sets of transmitted error conditions.

Description: z is a decimal number (0 or 1) which specifies:

0 - Primary transmit error set selected (default)
1 - Alternate transmit error set selected

See the D command for the types of errors included in the primary and alternate transmit error set. The Error Generation subsection gives a complete description of both the primary and alternate error types.

Example: The command sequence M1 would enable the alternate error set. An error code of 2 in all data lists transmitted thereafter would generate a dropped parity bit rather than an incorrect parity bit (also see Data command).

Command: P (Pattern Recognition)

Syntax: Pz

Purpose: The P (Pattern Recognition) command is an optional command, available only in the RT Simulator and Bus Monitor modes, which is used to program a pattern-recognition word. When the P command is programmed, the 73A-455 Module will not begin operation following a T (Trigger) command until a command or status word is received that matches the pattern-recognition word. Data word recognition is not available with this command.

Description: z is a 4-character hexadecimal string which defines the bit pattern (16 bits) of the received command word.

If the characters CLR are sent for the z string, the 73A-455 Module will disable the P command and will then receive and process the first command following a T command.

On power-up, or after receipt of a HALT command, z is set to CLR.

In the RT Simulator mode, it will begin collecting and responding with data. The P command is typically used to synchronize the 73A-455 Module with the 1553 data stream so that a desired sequence of responses will be given as a result of a bus controller's sequence of command words.

In the Bus Monitor mode, it will begin collecting data. The P command and the External Trigger Input give additional flexibility in determining when the start of 1553 bus data capture will begin.

Example: The command "PD020" would hold operation of the 73A-455 Module until a command word with the bit pattern 1101000000100000 was received (receive command word to RT 26 at subaddress 1 for 32 words).

Command: Q (Quit)

Syntax: Q

Purpose: The Q (Quit) command allows the system controller to terminate a bus communications sequence at any time. It also allows the ATE system controller to regain control of a 73A-455 Module that cannot finish its bus communication sequence because the unit under test (UUT) is not communicating with the 73A-455 Module.

Description: The Q command is the only way to terminate the Bus Monitor collection mode and still preserve the collected data. In the Bus Monitor or Remote Terminal mode, the Q command terminates bus activity as soon as a gap in data traffic occurs. It terminates bus activity in the Bus Controller mode at the time when the next message would have started.

Example: If a bus communications sequence is in progress, issuing the Q command to the 73A-455 Module will halt the bus communications sequence and resume command/response communications with the 73A-455 Module. All previously programmed card parameters such as Receiver Threshold Level, Response Time Gap Value, etc., will be unchanged. Any data programmed into buffers, or collected from the 1553 bus and stored into buffers, will also remain unchanged.

NOTE: The Q and K commands are the only commands that can be issued to the 73A-455 Module while a bus communications sequence is in progress to resume command/response communications with the 73A-455 Module. Any other commands sent during a bus communications sequence will be lost.

Command: R (RT Response Time List)

Syntax: $Rz_1,z_2;z_2;...z_2$

Purpose: The R (RT Response Time List) command is an optional command used only in the RT Simulator Mode. The R command associates a specific RT response time (other than the 4-μs default value) with each message received by the 73A-455 Module.

Description: Before the R command can be used, a B (Buffer) command must be issued to establish the size of the RT Response Time List buffer.

z_1 is a decimal number between 1 and the maximum number of possible entries in the RT Response Time List buffer as defined by the B command. z_1 defines the starting position in the RT Response Time List into which the first response time will be loaded.

z_2 represents the response time in microseconds to be entered into the RT Response Time List. z_2 may range in value from 4 to 65535.

The actual response time measured between the transition of the received parity bit and the mid-transition of the response sync pattern when programmed from 4 to 65,535 microseconds is nominally 4.25 to 65,535.25 microseconds. The accuracy of the crystal on the 73A-455 Module is 0.01%. For precise long response times, these two possible sources of error should be taken into account.

The R command can be used to generate a no-response condition by programming a value that would cause the response to occur as if responding to the following message. The response would originate from the transmit buffer associated with the last RT addressed. When using the R command in this manner, one less entry should be specified in the RT Response Time List for each response skipped.

Example: When more than one response-time entry is contained in the RT Response Time List, the next available response time from the list determines how long the 73A-455 Module will wait before responding to a bus controller command word.

If the R command R1,5;10;8;9 were issued, the response times associated with the first nine received bus controller commands would be:

Terminal Response

Command Word	Time Used
1st	5 µs
2nd	10 µs
3rd	8 µs
4th	9 µs
5th	5 µs
6th	10 µs
7th	8 µs
8th	9 µs
9th	5 µs

Note that the RT Response Time List applies to the order in which bus command words are received, and not to the RTs addressed to respond.

A BR4 Buffer Allocation command is required prior to the R command for the above example.

Command: S (Sequence List)

Syntax: $Sz_1,z_2[,z_3];z_2[,z_3];...z_2[,z_3]$

Purpose: The S (Sequence List) command is used in the Bus Controller Simulator Mode ONLY. The S command specifies the order in which transmit buffers will send their messages; the messages themselves are taken from the data list associated with each buffer.

The S command is also used to specify the "pace" interval, or time between messages transmitted by the 73A-455 Module. The pace interval is defined as the time between the last parity transition of one message and the first sync transition in the following message transmitted by the 73A-455 Module.

Description: z_1 is a decimal number from 1 to 30000 that specifies the location in the Bus Controller Sequence List where loading of buffer numbers is to begin.

z_2 is a decimal number from 0 to 31 that specifies the transmit buffer number to be loaded into the Sequence List.

z_3 is an optional parameter in the range of 14 to 65535 which specifies the pace interval in microseconds. If z_3 is not specified, the default value is 1000.

NOTE: The value of the z_3 parameter corresponding to a z_2 parameter specifies the interval prior to that message. To obtain the fastest response to an external trigger, the first z_3 in the message list should be set to 14.

When pace intervals of less than 1,000 microseconds are chosen, care must be taken to insure that the pace interval is long enough to allow for the RT response message plus the RT response time of the prior message. The following equation can be used to calculate the minimum z_3 pace interval:

$$z_3 = 20 (A + B + 2)$$

where:

A = total number of words including the status word in the RT response message

B = maximum RT response time in microseconds

If the pace interval is less than the minimum time specified in the above equation, a "data collision" on the 1553 bus may occur. A "data collision" will result in garbled data since two devices, the 73A-455 Module and the RT, will be transmitting at the same time. Whatever RT data is received prior to the data collision will be stored in the receive buffer.

Interval gaps of a minimum of 14 microseconds within a message can be generated as an error condition by specifying (in the data list in the D command) an end-of-message flag before the required number of words are sent, and specifying the buffer number twice in the S command. The second entry should have the pace value set to the desired gap duration between the two partial messages.

Example: To send messages from buffers 3, 8, 21, 3, and 9 in that order, the command sequence S1,3;8;21;3;9 would be used. The messages would be automatically paced at the default value of 1,000 microseconds. Later, to send the third message from buffer 16 instead of buffer 21, and to decrease the pace interval between the second and third messages to 670 microseconds, the command sequence S3,16,670 would be sent to the 73A-455 Module. This redefines the 3rd entry in the test only.

Command: T (Trigger)

Syntax: $Tz_1[,z_2]$

Purpose: The T (Trigger) command initiates a 1553 bus communications sequence.

Description: Bus Controller Simulator Mode:

z_1 specifies the number of times the Bus Controller Sequence List must be executed to complete a bus communications sequence. If z_1 is a decimal number between 1 and 32767, the entire Bus Controller Sequence List will be executed the number of times specified, beginning with the first entry in the list. If z_1 is an "*" (Octal 52), the 73A-455 Module will repeatedly execute the entire list until a K or Q command, or External Halt Input signal is received by the card.

If z_1 is the letter S followed by a number in the range 1 to 32767, then the 73A-455 Module will step through the Bus Controller Sequence List, counting messages, until the indicated number of messages has been processed. The first TS Command will begin counting with the first entry in the list. Subsequent TS commands will continue counting from the point where the previous command stopped.

z_2 is an optional parameter which enables or disables External Trigger Input, as follows:

z_2	External Trigger Input
0	Input disabled (default)
1	Input enabled - bus communications will not proceed until an External Trigger Input is received by the 73A-455 Module

RT Simulator Mode:

z_1 specifies the number of messages that must be processed by the 73A-455 Module to complete a bus communications sequence. If z_1 is a decimal number between 1 and 32767, the number of messages specified must be processed before the 73A-455 Module will complete the current bus communications sequence. If z_1 is an "*" (Octal 52), the 73A-455 Module will continuously process messages until a K or Q command, or External Halt Input signal is received by the card.

The z_2 parameter function is the same as described above for the Bus Controller Simulator Mode.

Bus Monitor Mode:

The z_1 parameter is optional in the Bus Monitor Mode. If z_1 is not present, the 73A-455 Module continuously collects bus traffic in its 30,000-word buffer, wrapping the buffer as necessary, and saving the last 30,000 words of data.

If z_1 is an F, the 73A-455 Module will collect only the first 30,000 words of bus traffic. If the F is followed by a number from 1 to 30000, a low-going TTL pulse will be output on the Position Identification Output pin after the corresponding buffer position has been filled. This pulse can be used to externally trigger an additional monitor card.

When the T command is issued in the Bus Monitor Mode, the 73A-455 Module begins continuously collecting 1553 bus data until a K or Q Command, or External Halt Input signal is received by the module. Or, if the TF command is sent, until 30000 words are collected.

The z_2 parameter function is the same as described above for the Bus Controller Simulator Mode. If the External Trigger Input is used, then the unused z_1 position must be indicated by a comma, i.e., T,1.

Using the Trigger Command:

When a bus communications sequence is initiated with a T (Trigger) command, internal control of the 73A-455 Module is passed from the module's Z80A microprocessor to the 1553 transmitter/receiver interface. After the transmitter/receiver has control of the 73A-455 Module, the card will not respond to any commands issued to it except for the Q (Quit), K (Kill), or an External Halt Input signal, until the bus communications sequence initiated by the T command is complete. If any command other than a Q, K, or Halt is issued to the card while a bus communications sequence is in progress, the 73A-455 Module will ignore the commands.

To avoid sending commands which will be ignored during a bus communications sequence, the 73A-455 Module's interrupt capability (I command) should be enabled before the T command is issued. With its interrupt enabled, the 73A-455 Module will generate a Request True event when the bus communications sequence is complete (generates an SRQ on IEEE-488 controlled systems), indicating that commands will be accepted.

The next command that is normally issued to the 73A-455 Module following a T command is an A or C command. To avoid having the command ignored, structure the system controller's software so that an A or C command is not issued to the 73A-455 Module until an interrupt is received.

Both the External Trigger and Pattern command conditionally trigger a card and can be active at the same time. Figure 455-5 shows the triggering hierarchy when the External Trigger Input and/or P command are used.

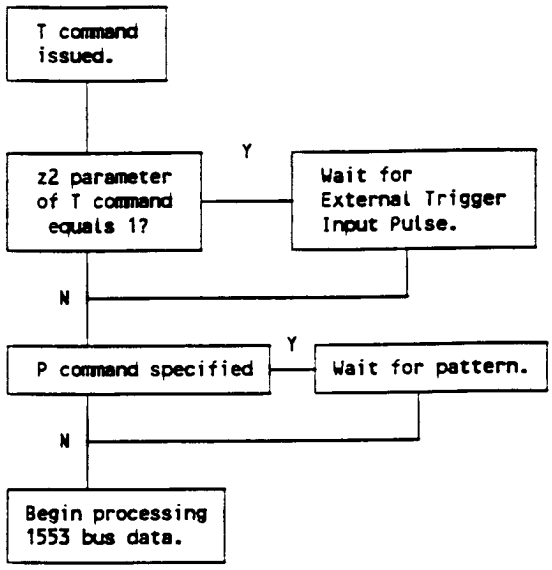


Figure 455-5: Triggering Hierarchy

The source for the external trigger is either pin 41 (pin 43 for channel B) of the DD50S connector on the front panel, or the VXIbus word serial command Trigger. The VXIbus Trigger command is typically generated by Group Execute Trigger in IEEE-488 controlled systems.

Examples: In the Bus Controller Simulator Mode, to execute the programmed Bus Controller Sequence List 27 times, the 73A-455 Module would be triggered using the command sequence T27. Following completion of the bus communications sequence, the first message to the first terminal in the Bus Controller Sequence List could be transmitted again by issuing the command T1.

If the 73A-455 Module was in the RT Simulator Mode and the command T326,1 was given, the module would wait for an external trigger, then respond to 326 command words by sending simulated RT messages to the controller for processing.

Command: V (Voltage)

Syntax: $Vz_1[,z_2]$

Purpose: The V (Voltage) command programs the 73A-455 Module's peak-to-peak transmit voltage level and receive voltage threshold level.

Description: When the peak-to-peak transmit voltage level is being programmed, z_1 is the character T followed by a 2- to 4-digit decimal number from 20 to 3440. The decimal number specifies the peak-to-peak transmit voltage level from 0.20V to 34.40V in 0.01V steps which are then rounded off to the nearest of up to 250 levels.

To program the receive voltage threshold level, z_1 is the character R followed by a decimal number in the range of 50 to 900. The decimal number specifies a peak-to-peak receive voltage threshold level of 0.50V to 9.00V in 0.01V steps rounded off to the nearest of up to 250 levels.

z_2 is optional, used with transmit voltage commands only. If used, it is a 2- to 4-digit number from 35 to 1000, which specifies the equivalent impedance at the 1553 bus interface, assuming a 55-ohm isolation impedance in each leg of the connection to the bus interface.

The voltages programmed by the V command are the peak-to-peak voltages occurring on a 1553 bus for a load of z_2 ohms for either a direct-coupled or transformer-coupled connection, as shown below. The voltage programmed by the V command corresponds to V volts peak-to-peak in the following diagram.

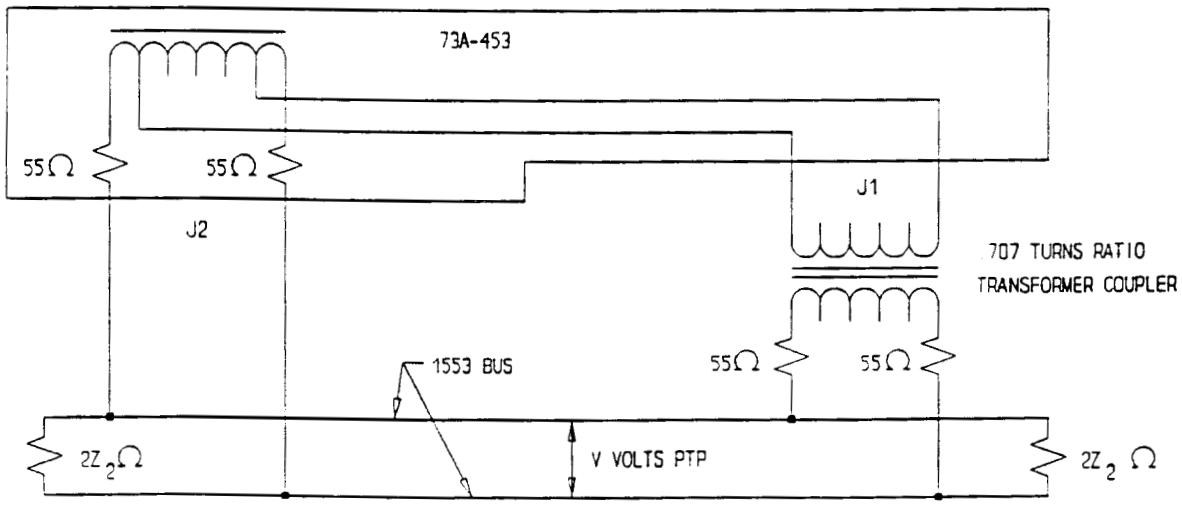


Figure 453-6: Direct- and Transformer-Coupled Circuit Connections

Approximate voltage ranges and nominal increment levels for some representative bus impedances are as follows:

Bus Impedance	Voltage Range
35 ohms	0.20 V to 8.20 V in 0.033 V ptp steps
70 ohms	0.30 V to 13.75 V in 0.055 V ptp steps
1000 ohms	0.75 V to 34.40 V in 0.138 V ptp steps

To determine approximate maximum output levels for other impedances than those listed above, use the formula:

$$V_{MAX} = 38.9z_2 / (z_2 + 132)$$

If an unacceptable voltage level is programmed with the V command, the ERR LED will light, and the command will be ignored. The default voltage will be programmed instead. The default voltage settings on power-up are a transmit level of 6.38 V ptp into 70 ohms and a 2.00 V ptp receive threshold level. Successful programming of the transmit or receive level may be checked with the E (Error) command.

For transformer coupled connections to the 73A-455, the voltage (V) specified is that which would result on the bus side of a coupler, as shown in Figure 455-6 above. The voltage at the transformer-coupled output (J2) of the 73A-455 Module is approximately $0.707Vz_2 / (110 + z_2)$.

The V command provides an easily programmable method of specifying the output level for various loads. The normal 1553 bus is loaded with two 70 ohm terminators, or 35 ohms. Waveform characteristics of the 73A-455 Module are not noticeably degraded for a 35-ohm to 1,000-ohm impedance range.

NOTE: The 73A-455 Module is not internally loaded, and a minimum load of 1000 ohms is usually required for proper operation.

For applications where electrical testing of a UUT is not being performed, it is recommended that a VT1375 or VT820,35 command be issued following the Function commands (FC or FR; Bus Controller or Remote Terminal). This will provide optimum transmit levels for protocol testing.

The optimum receive level is typically between 1.0 and 3.0V PTP (VR100 to VR300).

The receive level should not be set at the exact peak-to-peak value of the incoming signal. Since the 73A-455 Module looks for adequate signal above the programmed level, unreliable data transfer will occur if the receive level is programmed equal to the peak-to-peak value.

Example: The command sequence VT500,35 would program the transmit voltage level to 5.00V ptp, assuming a normal 1553 bus terminated at each end with 70 ohms. Using the command VR200 would set a receive voltage threshold level of 2.00V ptp.

CAUTION:

Connection of the 73A-455 Module's transformer-coupled outputs to anything other than a 1553 coupling transformer with isolation resistors on the bus interface side is NOT recommended, since there are no isolation resistors on the 73A-455 Module's transformer-coupled outputs to protect the circuitry against sustained bus collisions.

Command: TEST

Syntax: TEST

Purpose: The TEST command initiates the self test of PROM and RAM memory.

Description: The TEST sequence takes approximately 30 seconds to run. Test in progress is visually indicated by binary counting on five of the six LEDs at the top front of the module. The command must be issued for each channel to fully test the module.

The results of the test are obtained by issuing an input request to the module.

Result formats are as follows:

For a successful test: OK,Vx.x

Vx.x indicates the version and revision level of the firmware.

For a RAM error: RAM,xxxx-x,xx,xx

The arguments following RAM provide additional information on the failure (memory page and location within page).

For a PROM error: PROM,Uxx

This indicates that the single PROM memory device on the 73A-455 Module has failed. The Uxx argument has no meaning for the 73A-455.

Self test reports only the first error detected.

SYSFAIL, SELF TEST, AND INITIALIZATION

The 73A-455 Module will execute a self test of RAM and PROM for either channel on command. This module does not have a power-up self test.

A test can be run at any time during normal operation by using the TEST command. At the end of a test initiated by the TEST command, the module is restored to its pre-test state.

During a commanded self test or after a hard or soft reset:

1) SYSFAIL* is not asserted.

2) The module restores itself to its pre-test state. If the test fails, any error messages will be queued by the module for later reporting with the E command.

A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the 73A-455's commander, sets the Reset bit in the 73A-455's Control register and the Halt switch is ON.

The 73A-455 Module continuously monitors the +5V dc and ±24V dc power supplies. If all power supplies are valid, on power-up:

1) The SYSFAIL* (VME system-failure) line will never be set active, and the FAIL LED will not be lit. If any of the supplies fails, either at power-up or during operation, the SYSFAIL line will be set active and the FAIL LED will be lit and remain lit.

2) The module enters the VXIbus PASSED state (ready for normal operation) on power-up.

The default condition of each channel of the 73A-455 Module after the completion of power-up is:

Interrupt: Disabled (I command)
Transmit Level: 6.38V ptp (VT command)
Equivalent Bus Load for Transmit Level: 70 ohms (VT command)
Receive Threshold: 2.00V ptp (VR command)
Response Gap: 4 µs (R command)
Pace Interval: 1,000 µs (S command)
RT Response Time test value: 12 µs (G command)
Mode: Undefined (F command)
Pattern Trigger: Disabled (P command)
Error Mode: Primary error set selected (M command)
RT Response Time List: Unallocated (B command)
RT Sequence List: Unallocated (B command)
Transmit and Receive Buffers: Unallocated (B command)
High Speed Mode: Enabled (H command)
Transition Time Error Detection: Enabled (J command)
Request True interrupts disabled (these interrupts cause an SRQ on IEEE-488 systems).

SYSFAIL* Operation

SYSFAIL* becomes active if the module loses any of its power voltages. When the card cage Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the 73A-455 Module to deactivate SYSFAIL* in all cases except when +5 volt power is lost.

PROGRAMMING EXAMPLES

This section contains example programs which demonstrate how the various programmable features of the 73A-455 are

used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller. Additional examples are included in the Application Notes in Appendix E.

- **Definition of BASIC Commands**

The programming examples in this manual are written in Microsoft GW BASIC. These examples use the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

Command Result

CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)

The CALL ENTER statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the 73A-455.

CALL SEND (ADDRESS%, WRT$, STATUS%)

The CALL SEND statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.

END Terminates the program.

FOR/NEXT

Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.

GOSUB n

Runs the subroutine beginning with line n. EX: GOSUB 750 - runs the subroutine beginning on line 750. The end of the subroutine is delineated with a RETURN statement. When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.

GOTO n

Program branches to line n. EX: GOTO 320 - directs execution to continue at line 320.

IF/THEN

Sets up a conditional (IF/THEN) statement. Used with other commands, such as PRINT or GOTO, so that IF the stated condition is met, THEN the command following is effective. EX: IF I = 3 THEN GOTO 450 - will continue operation at line 450 when the value of variable I is 3.

REM

All characters following the REM command are not executed. REM statements are used for documentation and user instruction. EX: REM **CLOSE ISOLATION RELAYS**

RETURN

Ends a subroutine and returns operation to the line after the last executed GOSUB command.

- **Programming Examples In BASIC**

The following sample BASIC programs show how commands for one channel of the 73A-455 might be used. These examples assume that the 73A-455 Module is installed in a VXIbus card cage which is being controlled via an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 21 and to have converted the "A" channel's logical address to an IEEE-488 address of decimal 24 and the "B" channel's logical address to an IEEE-488 address of decimal 25.

Example 1:

The following example presents a program listing for programming the "A" channel of the 73A-455 Module as a Bus Controller in a Continuous Mode so that the resulting data stream can be viewed on an oscilloscope. Following that, a program is presented for programming one channel as a bus controller and a second channel or module as a remote terminal, handling a two-message sequence between them, and examining the received data in each module.

Lines 10 through 40 initialize the PC's IEEE-488 interface card as a system controller with an IEEE-488 address of decimal 21. Line 50 assigns the decimal IEEE-488 address of the 73A-455 to the variable ADDR455%.

```
10   DEF SEG = &HC400
         Defines memory location of IBM PC IEEE-488 Interface Module.
20   SEND = 9 : INIT = 0 : ENTER = 21
         Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
30   PC.ADDRESS% = 21 : CONTROL% = 0
         Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a
         controller.
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADDR455% = 24
         Define 73A-455's "A" channel IEEE-488 address.
60   CRLF$ = CHR$(13) + CHR$(10)
         Define a <CR> <LF> string.
70   WRT$ = "K" + CRLF$
80   CALL SEND(24, WRT$, STATUS%)
90   WRT$ = "FC" + CRLF$
100  CALL SEND(24, WRT$, STATUS%)
         Set the module to bus controller mode.
110  WRT$ = "BS2" + CRLF$
120  CALL SEND(24, WRT$, STATUS%)
         Allocate a two-word Bus Controller Sequence List buffer.
130  WRT$ = "S1,15:15,200:" + CRLF$
140  CALL SEND(24, WRT$, STATUS%)
         Load the Bus Controller Sequence List such that the two messages sent by the 455
         Module will be from the transmit buffer for RT#15, with the first message
         preceded by a 1000 µsec delay (default value) and the second preceded with a 200
         µsec delay.
```

```
150  WRT$ = "B15,R99" + CRLF$
160  CALL SEND(24, WRT$, STATUS%)
```

Allocate a 99-word receive buffer to store responses from RT#15.

NOTE: Any time either a transmit or receive buffer is allocated for an RT, both must be allocated for proper operation of the module.

```
170  WRT$ = "B15,T4" + CRLF$
180  CALL SEND(24, WRT$, STATUS%)
```

Allocate a 4-word transmit buffer for RT#15.

```
190  WRT$ = "D15,1,H,107C24:107822,1111,2222:" + CRLF$
200  CALL SEND(24, WRT$, STATUS%)
```

Load two messages in the transmit data list buffer for RT#15. The first message requests RT#15 to transmit 4 words. The second message requests RT#15 to receive 2 words of data whose hexadecimal contents are "1111" and "2222".

```
210  WRT$ = "T*" + CHR$(13)
220  CALL SEND(24, WRT$, STATUS%)
```

Trigger the 455 Module to continuously execute the Bus Controller Sequence List. Suppress line feed for the Trigger command.

Measure across Pins 2 and 15 of the front connector differentially using an oscilloscope with a suitable bus load. If the oscilloscope has a 50 ohm termination, it may be used.

The two messages should now be observable on the oscilloscope, separated by a 200 microsecond gap with 1 millisecond between successive message pairs. The peak-to-peak amplitude of the signal will be about 6.38 V ptp for a 70 ohm bus load, ranging down to 3.2 V ptp for a 35 ohm load or up to about 16 V ptp for a 1000 ohm bus load.

Example 2:

The following program listing shows how the second channel can be set up as RT#15 to respond to messages sent from the first channel. The two command messages are sent one time and the received data in each channel's receive buffer is examined.

Lines 10 through 40 initialize the PC's IEEE-488 interface card as a system controller with an IEEE-488 address of decimal 21. Line 50 assigns the decimal IEEE-488 address of the first channel to the variable ADDR455%. Line 60 assigns the second channel an IEEE-488 address of 25, using the variable BDDR455%.

```
10   DEF SEG = &HC400
```

Defines memory location of IBM PC IEEE-488 Interface Module.

```
20   SEND = 9 : INIT = 0 : ENTER = 21
```

Initialize PROM offsets for IBM PC IEEE-488 Interface Module.

```
30   PC.ADDRESS% = 21 : CONTROL% = 0
```

Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a controller.

```
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADDR455% = 24
```

Define "A" channel's IEEE-488 address.

```
60   BDDR455% = 25
         Define the "B" channel's IEEE-488 address.
70   CRLF$ = CHR$(13) + CHR$(10)
90   WRT$ = "K" + CRLF$
100  CALL SEND(BDDR455%, WRT$, STATUS%)
110  WRT$ = "FR" + CRLF$
120  CALL SEND(BDDR455%, WRT$, STATUS%)
         Reset the second channel and program it as a remote terminal.
130  WRT$ = "B15,R99" + CRLF$
140  CALL SEND(BDDR455%, WRT$, STATUS%)
         Allocate a 99-word receive buffer for RT address 15.
150  WRT$ = "B15,T6" + CRLF$
160  CALL SEND(BDDR455%, WRT$, STATUS%)
         Allocate a 6-word transmit buffer for RT address 15.
170  WRT$ = "D15,1,H,107800,3333,4444,5555,6666:107800:" + CRLF$
180  CALL SEND(BDDR455%, WRT$, STATUS%)
         Define status word and four data words for first message; define status word for
         second message.
190  WRT$ = "T2" + CHR$(13)
200  CALL SEND(BDDR455%, WRT$, STATUS%)
         Program module to accept and respond to 2 messages
210  WRT$ = "K" + CRLF$
220  CALL SEND(ADDR455%, WRT$, STATUS%)
230  WRT$ = "FC" + CRLF$
240  CALL SEND(ADDR455%, WRT$, STATUS%)
         Program the first channel as a bus controller the same as in the preceding example.
250  WRT$ = "BS2" + CRLF$
260  CALL SEND(ADDR455%, WRT$, STATUS%)
270  WRT$ = "S1,15:15,200:" + CRLF$
280  CALL SEND(ADDR455%, WRT$, STATUS%)
290  WRT$ = "B15,R99" + CRLF$
300  CALL SEND(ADDR455%, WRT$, STATUS%)
310  WRT$ = "B15,T4" + CRLF$
320  CALL SEND(ADDR455%, WRT$, STATUS%)
330  WRT$ = "D15,1,H,107C24:107822,1111,2222:" + CRLF$
340  CALL SEND(ADDR455%, WRT$, STATUS%)
350  WRT$ = "T1" + CHR$(13)
360  CALL SEND(ADDR455%, WRT$, STATUS%)
         Send the two-message sequence one time.
370  WRT$ = "A15,1,HF" + CRLF$
380  CALL SEND(ADDR455%, WRT$, STATUS%)
         Program the first channel to return RT 15's response data.
390  FOR I = 1 TO 9
400  RD$ = SPACE$(25)
410  CALL ENTER(RD$, LENGTH%, ADDR455%, STATUS%): PRINT RD$
420  NEXT I
         Print first 9 words in receive buffer.
430  WRT$ = "A15,1,HF" + CRLF$
440  CALL SEND(BDDR455%, WRT$, STATUS%)
         Program RT module (second channel) to look at data received from bus controller
         module.
```

```
450  FOR I = 1 TO 5
460  RD$ = SPACE$(25)
470  CALL ENTER(RD$, LENGTH%, BDDR455%, STATUS%): PRINT RD$
480  NEXT I
          Print first 5 words in buffer.
490  STOP
```

The printout for the bus controller module includes the two command words sent out. They are stored by the 73A-455 Module in the receive buffer as part of its normal function to allow correlation of commands with responses. The printout of the nine words from the bus controller receive buffer should be as follows:

107C24	First bus controller command word
107800	RT status word
003333	RT data words
004444	
005555	
006666	
107822	Second bus controller command word
107800	RT status word
0B0000	No more data

The printout of the five words from the RT receive buffer should be as follows:

107C24	First bus controller command word
107822	Second bus controller command word
001111	Bus controller data words
002222	
0B0000	No more data

APPENDIX A - VXIbus OPERATION

The 73A-455 Module is a C size single slot VXIbus Message-Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The 73A-455 Module is neither a VXIbus commander or VMEbus master, and therefore it does not have a VXIbus signal register. The 73A-455 is a VXIbus message based servant.

The module supports the Normal Transfer mode of the VXIbus, using the Write Ready and Read Ready bits of the module's Response register.

A Normal Transfer mode read of the 73A-455 Module proceeds as follows:

1. The commander reads the 73A-455's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready bit until it becomes true.

2. The commander writes the Byte Request command (0DEFFh) to the 73A-455's Data Low register.

3. The commander reads the 73A-455's Response register and checks if the Read Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Read Ready bit until it becomes true.

4. The commander reads the 73A-455's Data Low register.

A Normal Transfer mode write to the 73A-455 Module proceeds as follows:

1. The commander reads the 73A-455's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready bit until it becomes true.

2. The commander writes the Byte Available command (0BCXX or 0BDXX, depending on the End bit) to the 73A-455's Data Low register.

The 73A-455 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the 73A-455's address space may cause incorrect operation of the module.

CAUTION:

If the user's card cage has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR* (as defined by the VXIbus Specification) may cause operating problems on these boards.

As with all VXIbus devices, the 73A-455 Module has registers located within a 64 byte block in the A16 address space.

The base address of the 73A-455 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches.

73A-455 Configuration Registers

Below is a list of the 73A-455 Configuration Registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The address is relative to the module's base address.

REGISTER DEFINITIONS

Register	Address	Type	Value (Bits 15-0)
ID Register	0000H	RO	1011 1111 1111 1100 (BFFCh)
Device Type	0002H	RO	See Device Type definition below
Status	0004H	R	1X11 1111 1111 1111 (BFFFh or FFFFh)
Control	0004H	W	0111 1111 1111 110X (7FFCh or 7FFDh)
Offset	0006H	WO	Not used
Protocol	0008H	RO	1111 1111 1111 1111 (FFFFh)
Response	000AH	RO	Defined by state of the interface
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below
Data Low	000EH	R	See Data Low definition below

BIT DEFINITIONS

Register	Bit Location	Bit Usage	73A-455 Value	73A-455 Usage
ID	15-14	Device Class	10	Message Based
	13-12	Address Space	11	A16 only
	11-0	Manufact. ID	1111 1111 1100	Colorado Data Systems
Device Type	15-0	Device Type	1111 1110 0011 1000	Ones comp. of 455
Status	15	A24/32 Active	1	Not used
	14	MODID*	1	MODID line not active
			0	MODID line active
	13-4	Device dependent	11 1111 1111	Not used
	3	Extended*	1	Not used
	2	Passed	1	Always passed
	1-0	Device dependent	11	Not used

BIT DEFINITIONS (continued)

Register	Bit Location	Bit Usage	73A-455 Value	73A-455 Usage
Control	15	A24/32 Enable	1 or 0	Not used
	14-2	Device dependent	111 1111 1111 11	Not used
	1	SYSFAIL Inhibit	1	Disables module from driving Sysfail
			0	Enables module to drive Sysfail
	0	Reset	1	Reset
			0	Not reset
Protocol	15	CMDR*	1	Servant only
	14	Signal Reg.*	1	No Signal Reg.
	13	Master*	1	Slave only
	12	Interrupter	1	Interrupter
	11	FHS*	1	No Fast Handshake capability
	10	Shared Memory*	1	No Shared Memory capability
	9-4	Reserved	11 1111	Not used
	3-0	Device dependent	1111	Not used
Response	15	Defined value of 0	0	Per VXI
	14	Reserved	1	Per VXI
	13	DOR	1	Data Output Ready
	12	DIR	1	Data Input Ready
	11	ERR*	1	Not used
	10	Read Ready	1 or 0	Indicates that the instrument portion of the module has data available to be read. Set by the instrument following a "Byte Request" command, and cleared on a read from the Data Low register or on reset.
Response	9	Write Ready	1 or 0	Cleared upon receipt of a "Byte Available" command. Set when the instrument is ready to receive a data byte or on reset.
	8	FHS Active*	1	Not used
	7	Locked*	1	Not used
	6-0	Device dependent	111 1111	Not used

Data High - not implemented.

Data Low Register

The Data Low register is used to send the 16-bit VXI Word Serial commands and read the response to those commands, as required. The Word Serial commands supported by the 73A-455 are:

Begin Normal Operation - begin operation of the module.

Byte Available - the Word Serial command which contains the module-specific command and data bytes used to operate the 73A-455 Module. Command/data information is contained in the least significant eight bits of the 16 bit command.

Byte Request - the Word Serial command sent to the 73A-455 Module before reading response data and status (the response to the Accept or Error commands, for example). The data is returned in bits 7-0. Bit 8 is set for end-of-message.

Clear - clears the VXIbus interface and any pending commands.

Trigger - triggers the 73A-455 Module for communication on the MIL-STD-1553 bus, assuming the module has been properly programmed and armed for external trigger operation by the T command.

Read Protocol - reads the VXIbus protocol of the 73A-455. The response is read from the Data Low register and returns the following bit arguments and contents:

VXIbus Version Level:

Bit	15
	0 VXIbus Version 1.2 Device

Device dependent (unused):

Bits	14	13	12	11
	1	1	1	1

Reserved:

Bits	10	9	8	7	6	5
	1	1	1	1	1	1

Triggered*: (supports trigger command)

Bit	4
	1 This module does not support trigger command.

I4*: (supports VXIbus 488.2 Instrument protocol)

Bit	3
	1 This module does not support 488.2 protocol.

I*: (supports VXIbus Instrument protocol)

Bit 2

0 This module supports instrument protocol.

ELW*: (supports Extended Longword Serial protocol)

Bit 1

1 This module does not support ELW protocol.

LW*: (supports Longword Serial protocol)

Bit 0

1 This module does not support LW protocol.

73A-455 Interrupts

The 73A-455 will interrupt its commander with the following "event" if it does not recognize a VXIbus Word Serial command:

Unrecognized Command Event:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 1  1  1  0  1  1  1  1  <--Logical Address--->
```

This event is generated by this module in response to any command sent to the data low register other than the following:

Byte Available Command
Byte Request Command
Begin Normal Operation Command
Clear Command
Read Protocol Command
Trigger Command

Request True:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 1  1  1  1  1  1  0  1  <--Logical Address--->
```

This event is generated as programmed by the I command.

APPENDIX B - INPUT/OUTPUT CONNECTIONS

Four TNC Triax female connectors are provided at the top of the front panel. The top two connectors, XFMR A and XFMR B are for transformer-coupled connections to the MIL-STD-1553 Bus A and B. The lower two connectors, DIR A and DIR B, are for direct-coupled connection to the MIL-STD-1553 Bus A and B. Install cabled TNC Triax male connectors to one of these connector sets.

The bottom 50 pin DD50S connector labeled S4 is used to provide the interface to the optional I/O signals for channel A and B. A 73A-782P Hooded Connector is the required mating connector. It is recommended that you wire only those signals to be used. The transformer- and direct-coupled MIL-STD-1553 bus connections are also available on the DD50S connector as an alternative to the triax connectors. However, on-board jumpers can be cut to disconnect these four connections if desired. Consult the factory for information (1-800-CDS-ATE1).

The signal assignments for the DD50S Connector are listed below. The channel A pin number is shown first, and the channel B pin number is second. When viewing the connector from the front, pin 1 is on the bottom right, and pin 50 is on the top left.

Pin Number A, B	Signal
18, 33	Common Mode Voltage Input.
1, 17	1553 Direct-Coupled Bus High
34, 50	1553 Direct-Coupled Bus Low
2, 16	1553 Transformer-Coupled Bus High
19, 32	1553 Transformer-Coupled Bus Low
7, 11	External Clock Input, TTL, 16 times 1553 data rate, will drive 1 TTL load.
21, 30	Transmit/Reconstructed Receive Clock Output, TTL, will drive 6 LSTTL loads.
8, 10	Data Bus Input Active Output, open collector, 10K pull up, 5 mA sink capability.
39, 45	Position Identification Output, TTL, Low True, 0.5 µs minimum width, will drive 6 LSTTL loads.
6, 12	Pattern Recognition Output, will drive 10 LSTTL loads, Low True.
41, 43	External Trigger Input, TTL, Low True, Minimum pulse 50 ns width.
22, 29	Transmitted Data High Output, TTL, Manchester bi-phase, Low True, Serial, will drive 6 LSTTL loads.
38, 46	Transmitted Data Low Output, TTL, Manchester bi-phase, Low True, Serial, will drive 6 LSTTL loads.
5, 13	Reconstructed Received Data Low Output, TTL, Manchester bi-phase, Low True, Serial, will drive 4 LSTTL loads. Data is valid on rising edge of reconstructed clock (pin 21, 30).
24, 27	Data Word Received Output, TTL, 1 µs high pulse at end of each received word, will drive 6 LSTTL loads.
23, 28	Message Error Output, TTL, Low True, 125 ns width, minimum, will drive 10 LSTTL loads.
40, 44	External Halt Input, TTL, Low True, Minimum pulse 50 ns width.
3, 9, 15, 20, 31, 42:	Digital Ground.
35, 49	Analog ground. Return for Common Mode Voltage Input.
36, 37, 47, 48:	Analog ground.
25, 26	Reserved.

Common Mode Voltage Input (Pins 18, 33)

The Common Mode Voltage Input allows injection of a common-mode voltage onto the 1553 data bus. Maximum input level is ±11V dc to 2 MHz.

1553 Bus Signals (Direct Coupled - Pins 1, 17, 34, 50; Transformer Coupled - Pins 2, 16, 19, 32)

Direct-coupled and transformer-coupled 1553 data bus signals.

External Clock Input (Pins 7, 11)

The External Clock Input varies the 1553 data bus bit rate by supplying an external clock signal. The external clock signal must be provided at a frequency of sixteen times the desired 1553 data bus bit rate. The external clock may vary between 15 MHz and 17 MHz, resulting in a 937.5 KHz to 1.0625 MHz bit rate on the 1553 data bus.

Transmitter/Reconstructed Received Data/Clock Output (Pins 21, 30)

This output provides a 1 MHz clock for both transmitted and received data. This clock synchronizes itself to each new received data input. The next transmission of data is then synchronous with that clock. The clock is active at all times.

The clock transitions positive approximately 75 nsec prior to the mid-bit transition of the TTL Transmit Data Outputs (pins 22, 29, 38, and 46) and the TTL Reconstructed Receive Data output (pins 5, 13).

Data Bus Input Active Output (Pins 8, 10)

The Data Bus Input Active is an output that is active high to indicate that data is being received by the 73A-455 Module.

The Data Bus Input Active outputs from more than one 73A-455 output channel may be connected together and will indicate an active high only if all modules so connected are simultaneously receiving data. The output may be used for detection of simultaneous transmission in dual-redundant bus systems.

Position Identification Output (Pins 39, 45)

The Position Identification Output provides a low TTL pulse associated with any specified transmit word in either the Bus Controller Simulator or RT Simulator Mode (see the D command). The width of this pulse is between 62.5 and 450 microseconds. The pulse will occur during the sync pattern of the transmitted word following the specified transmit word for the same RT. This output is useful for triggering an oscilloscope in a large, repeating message sequence.

The Position Identification Output also provides a low TTL pulse at any one specified position in the bus monitor collection buffer. In the Bus Monitor Mode, this output can be used to indicate memory is nearly full and to externally trigger data collection on another 73A-455 Module programmed to the Bus Monitor Mode (see Applications Note 455-III).

Pattern Recognition Output (Pins 6, 12)

This output is used when the 73A-455 Module is in the RT Simulator Mode or the Bus Monitor Mode. The output will be set low when a received command word matches the 16-bit word programmed by the P command. It will remain low until a new bus transaction sequence is initiated with the T command.

External Trigger Input (Pins 41, 43)

The External Trigger Input is only active when the z_2 parameter of the T command is a 1. In this case, the 73A-455 Module will not initiate a 1553 bus communications sequence until an External Trigger Input is received on this pin or a VXIbus Trigger command is sent. After receiving the External Trigger Input signal, the 73A-455 Module will begin communication on the 1553 bus within 100 microseconds. Repeatability of the time interval is ±3.5 microseconds.

Transmitted Data High Output (Pins 22, 29)
This TTL output is active low for a transmitted high level on the 1553 bus. It is at an inactive high a) when the module is transmitting a low level on the bus, or b) if this module is receiving data, or c) the bus is inactive.

This output is a TTL version of the actual analog transmit level and reflects the Manchester bi-phase data and parity format, and includes the sync patterns. The actual analog output is delayed by about 100 nanoseconds from this TTL output. The 1 MHz Transmit Clock Output (pins 21, 30) transitions positive approximately 75 nanoseconds prior to the mid-bit transition of this signal.

Transmitted Data Low Output (Pins 38, 46)
This TTL output is active low for a transmitted low level on the 1553 bus. It is at an inactive high a) when the module is transmitting a high level on the bus, or b) if this module is receiving data, or c) the bus is inactive.

This output is a TTL version of the actual analog transmit level and reflects the Manchester bi-phase data and parity format, and includes the sync patterns. The actual analog output is delayed by about 100 nanoseconds from this TTL output. The 1 MHz Transmit Clock Output (pins 21, 30) transitions positive approximately 75 nanoseconds prior to the mid-bit transition of this signal.

Reconstructed Received Data Low Output (Pins 5, 13)
This output provides a TTL representation of the received data including the sync pattern and Manchester bi-phase data and parity bits. This output is active low for a low receive level on the bus. It is inactive high for a high receive level, or if this module is transmitting or if the bus is inactive. The 1 MHz Reconstructed Receive Clock Output (pins 21, 30) synchronizes to this incoming signal and transitions high approximately 75 nanoseconds prior to the mid-bit transition of this signal.

Data Word Received Output (Pins 24, 27)
The Data Word Received Output generates a 1-microsecond TTL high pulse each time a command, status, or data word is received. This output is active in the Bus Controller Simulator, RT Simulator, and Bus Monitor Modes.

Message Error Output (Pins 23, 28)
The Message Error Output is only active when the 73A-455 Module is functioning as a bus controller. The Message Error Output line will pulse low each time a status word is received with bit 6 (Message Error) set.

External Halt Input (Pins 40, 44)
The External Halt Input is used to terminate a 1553 bus communications sequence. When a halt input is received, the 73A-455 Module will terminate 1553 bus communications and accept additional programming commands. This input is the hardware equivalent of the Q command. The External Halt Input signal will be examined, and the halt request honored, as described for the Q command.

APPENDIX C - VXIbus GLOSSARY

Certain terms used in this manual have very specific meanings in the context of a VXIbus System. A list of these terms is presented below.

Commander

A VXIbus device that has bus master capability and has VXIbus servants under it in the system hierarchy. A commander may be a servant as well.

Fast Handshake

Compared to the Normal Transfer Mode of the VXIbus, the Fast Handshake Transfer Mode reduces the number of VMEbus data transfer cycles by 50%. Upon receipt of a request for data, a fast handshake module is able to return data in less than 20 µs, so that the VXIbus fast handshake protocol can be used by the module's commander. Using fast handshake protocol, data can be written and read without checking the Ready bits in the module's Response register.

Hard Reset

This is the state of the module when the SYSRESET* line is true. While in this state, the module is inactive and its Status and Control registers are cleared. The SYSFAIL* line is driven low, and the Failed LED is lit. In the case of a CDS 73A-IBX card cage, for example, a module hard reset occurs when the card cage is powered-up or the Reset switch on the front panel of the 73A-151 Resource Manager/IEEE-488 Interface Module is depressed.

Interrupt Handler

The module in the VXIbus system that generates the hardware interrupt acknowledge for a particular VME interrupt level. The software interrupt handler may or may not be on the same module as the hardware interrupt handler. In the case of CDS instrument modules, both the hardware and software interrupt handlers reside on the commander module of a given servant module.

Logical Address

A unique eight bit number which identifies each VXIbus device in a system. It defines the device's A16 register addresses, and indicates the device's commander/servant relationship.

Reset Bit

Bit 0 in the Control register of the module. When set to a one (1) by the module's commander or resource manager, the device is forced into a reset state.

Resource Manager

A message based commander located at logical address 0, which provides configuration management services, including self test, address map configuration, commander/servant mapping, and diagnostic management. In CDS systems, the Resource Manager function is co-located with the VMEbus controller, the slot 0 timing functions, and the system controller interface.

Servant

A VXIbus device that may or may not have bus master capability, that is under control of a commander in the VXIbus system hierarchy. A servant may also be a commander.

Soft Reset

This state is entered when the Reset bit in the module's Control register is set to one (1) by the module's commander. While in this state, a device is inactive, interrupts which are pending are unasserted, all pending bus requests are unasserted, and the onboard processor is halted. The device's VMEbus slave interface is active in this state; however, the device is incapable of responding to any commands other than RESET and SYSFAIL INHIBIT. In the case of a CDS 73A-IBX Card Cage, for example, a module soft reset occurs when the card cage's 73A-151 Resource Manager/IEEE 488 Interface Module receives a STOP command over the IEEE-488 bus that is addressed to the 73A-455.

SYSFAIL INHIBIT

Bit 1 in the Control register of the module. When set to a one (1) by the VXIbus Resource Manager, the device is disabled from driving the SYSFAIL* line. CDS modules are designed so that the Sysfail Inhibit bit will work under all conditions except when the +5V power is lost.

VXI Commands

These are commands passed from a commander to a servant within the VXIbus environment. A command may or may not be prompted by an external event. For example, an IEEE-488 GROUP EXECUTE TRIGGER will generate a Trigger command to all addressed devices. However, a BEGIN NORMAL OPERATIONS command is generated by the VXIbus resource manager and has no external source.

VXI Events

Events are passed from a servant to a commander. They may be generated by the servant either in response to a command (for example, Unrecognized Command event) or due to a condition detected in the module (internal error).

VXI Message Based Instrument

An intelligent instrument that implements the defined VXIbus registers and, at a minimum, the word serial protocol. All CDS instruments are message based.

VXI Word Serial Protocol

The simplest required communication protocol supported by Message Based devices in a VXIbus system. It utilizes the A16 communications registers to transfer data using a simple polling handshake method. All CDS instruments implement the word serial protocol.

488-VXIbus Interface

An IEEE-488 to VXIbus Interface Device is a message based device which provides communication between the IEEE-488 bus and VXIbus instruments.

APPENDIX D - APPLICATION NOTES

APPLICATION NOTE

SIMULATING DUAL REDUNDANT BUS CONTROLLERS

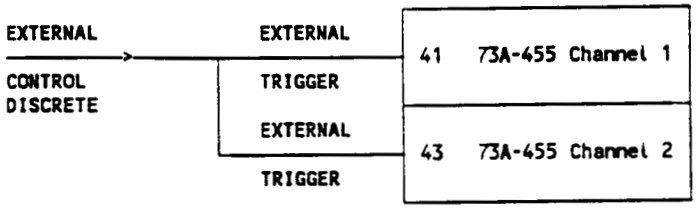
The two channels of the same 73A-455 Module can be used to simulate a dual redundant MIL-STD-1553 Bus Controller. The techniques described below can be extended to three or four 73A-455 channels to handle triple- or quad-redundant Bus Controller applications.

The 73A-455 Module is programmed by ASCII character strings from a calculator, computer or some other type of controller. The 73A-455 Module contains an on-board microprocessor which does some setup compatibility tests of the buffer allocation, sequence, and data commands before it allows transmission on the 1553 bus in response to a T Command. Since the time it takes to perform these checks is application dependent, it is difficult to time the start or completion of one module's operation with respect to an event on the other module totally through software control.

For this reason, an external front connector 73A-455 Module input is provided for each channel to aid in this timing control.

Pins 41 and 43 are external trigger inputs that will trigger a 73A-455 Module that has been preloaded with data and triggered with an external trigger option of the T Command. Transmission will start a minimum of 100 microseconds after the active low input has been applied. Transmission initiation can be programmed for longer times by setting the pace value for the first message in the sequence command to longer than the minimum 14 microsecond value. There is an uncertainty of ±3.5 microseconds in the trigger time.

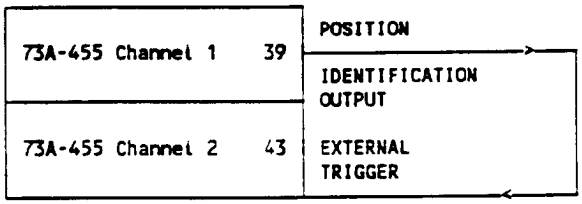
An external discrete may therefore be used to halt one channel and start the next channel with a delay time repeatability of ±3.5 microseconds.



A second method of transferring control from one channel to another involves using a known event on the first channel to trigger the second channel. This is accomplished by transmitting a finite message sequence on the first channel and using an output of that channel called the position identification output (Pin 39, A channel; Pin 45, B channel). A low TTL pulse may be output on this pin on a software specified word near the end of the transmit list using a capability of the D Command.

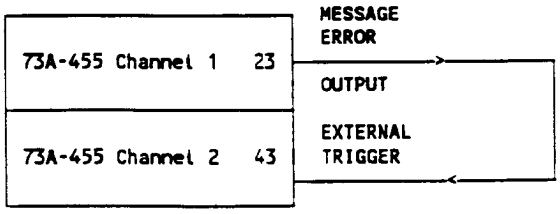
This output can be connected to the external trigger input of the second channel. Using the timing control technique described above, the second channel's transmission can follow an event in the first channel's transmission by 100 microseconds or more with a delay time repeatability of ±3.5 microseconds. By programming the position identification pulse to occur at least 100 microseconds before the second channel's desired starting time, this allows programming the second channel to start within 4 microseconds of some event on the first channel.

An application of this would be to experimentally program the delay between the first and second channels to the desired point, using an oscilloscope. Because of the ±3.5 microsecond random uncertainty in triggering the second channel, running this test many times allows testing a dual redundant RT's response to a superceding command with a 7 microsecond uncertainty. The uncertainty and randomness of the delay is an excellent test of an RT's superceding command operation.



A third method for triggering the channel uses the message error bit returned in the status word by a remote terminal. The 73A-455 Module contains a hardware output that supplies a low pulse any time the status word message error bit is detected by the module, when in the Bus Controller Mode. This output is useful for testing transfer of an RT to its redundant bus following an error transmitted by the bus controller.

For example, if an RT detects an error (such as Manchester error or parity error) on a data word following a valid command word, the RT will not respond to the command error, and sets the message error bit in response to a transmit status mode code in the following command. The first channel of the 73A-455 Module can be programmed as a bus controller to output a data error followed by a request for status mode code. When the status word comes back with the message error bit set, the message error bit output can be used to trigger the second channel to transmit. The second channel's transmission can be programmed to follow the status word message error bit detection a minimum of 100 microseconds later with a predictability of ±3.5 microseconds.



APPLICATION NOTE

BUS MONITOR MODULE CHAINING

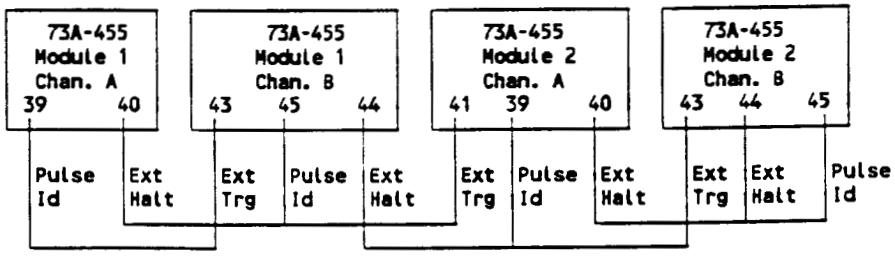
The 73A-455 Module provides a trigger command capability to output a position identification output (pin 39 on channel A, pin 43 on channel B) which will output a low TTL pulse at a user-specified position in the 30000-word bus monitor receive buffer, and a command to stop data collection after the 30000 word buffer is full. This output can be used to trigger an already set up additional monitor module through its external trigger input.

The external trigger input takes approximately 70 microseconds after being activated before collection of data starts. Collection of data also does not start until a word with a command sync pattern appears on the bus. To guarantee that no data is missed during transfer from one module to another, the maximum message length of 33 words plus an additional 4 words to accommodate the 70 microseconds must be still collected on the first module following the output of the position identification pulse. This means the position identification pulse should be programmed at least 33 words before the end of the 30000 word buffer.

The 73A-455 Module in the Bus Monitor Mode requires a Q command or external halt input to take it out of the Bus Communication Mode so that the system controller can read the data from the module. The module does not indicate to the system controller when it is full. Using the Q command is not practical unless some means is available of knowing when the module will be full and providing compatible software timing.

The best way of taking the Bus Monitor off the bus is to connect the external halt pin of the module to the position identification pulse of the next module in the chain. This ensures that the receiver on the module will not be deactivated until the next module has started collection. For the last module in the chain, the module's position identification output may be connected to its own external halt input.

In the following diagram, both channels of each of two 73A-455 Modules are connected to make a 120,000 word buffer.



The following example would program triggering and data collection on the above two modules. The program assumes the four instruments on the two modules have IEEE-488 addresses of 24 and 25 for channels A and B of module 1, and 26 and 27 for channels A and B of module 2.

Lines 10 through 40 initialize the PC's IEEE-488 interface module as a system controller with an IEEE-488 address of decimal 21.

```
10   DEF SEG = &HC400
         Defines memory location of IBM PC IEEE-488 Interface Module.
20   SEND = 9 : INIT = 0 : ENTER = 21
         Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
30   PC.ADDRESS% = 21 : CONTROL% = 0
         Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a
         controller.
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADR1% = 24
60   ADR2% = 25
70   ADR3% = 26
80   ADR4% = 27
         Assign IEEE-488 addresses of 24, 25, 26, and 27 for the four channels.
90   WRT$ = "K" + CHR$(13)
100  CALL SEND(ADR1%, WRT$, STATUS%)
110  WRT$ = "FM" + CHR$(13)
120  CALL SEND(ADR1%, WRT$, STATUS%)
130  WRT$ = "K" + CHR$(13)
140  CALL SEND(ADR2%, WRT$, STATUS%)
150  WRT$ =  "FM" + CHR$(13)
160  CALL SEND(ADR2%, WRT$, STATUS%)
170  WRT$ = "K" + CHR$(13)
180  CALL SEND(ADR3%, WRT$, STATUS%)
190  WRT$ =  "FM" + CHR$(13)
200  CALL SEND(ADR3%, WRT$, STATUS%)
210  WRT$ = "K" + CHR$(13)
220  CALL SEND(ADR4%, WRT$, STATUS%)
230  WRT$ =  "FM" + CHR$(13)
240  CALL SEND(ADR4%, WRT$, STATUS%)
         Reset and program all four channels to bus monitor mode. This program initializes
         the four channels in parallel.
250  WRT$ = "PXXXX" + CHR$(13)
260  CALL SEND(ADR1%, WRT$, STATUS%)
         Optional command to start collection at a user-specified command word pattern.
270  WRT$ = "TF29900" + CHR$(13)
280  CALL SEND(ADR1%, WRT$, STATUS%)
290  WRT$ = "TF29900,1" + CHR$(13)
300  CALL SEND(ADR2%, WRT$, STATUS%)
310  WRT$ = "TF29900,1" + CHR$(13)
320  CALL SEND(ADR3%, WRT$, STATUS%)
330  WRT$ = "TF29900,1" + CHR$(13)
```

```
340  CALL SEND(ADR4%, WRT$, STATUS%)
         Program first channel to start collection, putting a position identification pulse on
         the 29,900th word. Channels 2 through 4 are also programmed to start based on the
         external trigger.
350  WRT$ = "A,1,H" + CHR$(13)
360  CALL SEND(ADR1%, WRT$, STATUS%)
         Start collection on channel 1 when the module has been externally halted.
370  FOR I = 1 TO 30000
380  RD$ = SPACE$ (255)
390  CALL ENTER(RD$, LENGTH%, ADR1%, STATUS%)
400  GOSUB "STORE"
         User subroutine to utilize data as desired.
410  NEXT I
         Repeat for 30000 words.
420  WRT$ = "A,1,H" + CHR$(13)
430  CALL SEND(ADR2%, WRT$, STATUS%)
440  FOR I = 1 TO 30000
450  WRT$ = SPACE$ (255)
460  CALL ENTER(WRT$, LENGTH%, ADR2%, STATUS%)
470  GOSUB "STORE"
480  NEXT I
         . Repeat for channel 2.
         .
         .
         Repeat lines 420 to 480 for channels 3 and 4.
490  STOP
```

PING-PONGING BUS MONITOR CHANNELS

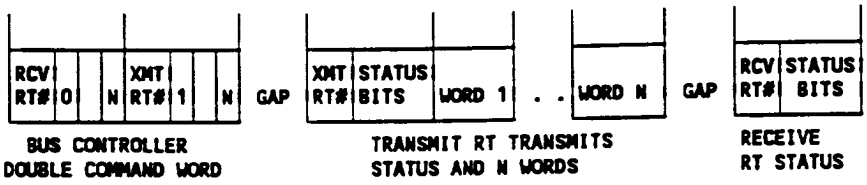
Ping-ponging the 73A-455 Module channel A and channel B inputs as bus monitors for continuous data collection is usually not practical because of limitations in the 73A-455 module-to-system controller transfer rate. In the Binary Read Mode, the 73A-455 Module is capable of returning one 1553 word (3 bytes) in 556 microseconds (depending on the system controller).

The 1553 bus traffic must occur at less than 1 word per 550 measurements to get one channel's responses back to the system controller while the other channel is filling up with present data bus traffic.

APPLICATION NOTE

RT-TO-RT TRANSFERS

This application note describes the programming of one channel of a 73A-455 Module as the Bus Controller, transmitting RT, or the receiving RT in an RT-to-RT transfer. The format of an RT-to-RT transfer on the MIL-STD-1553 bus is as follows:



The following program lists the commands that would be sent to a 73A-455 Module channel simulating RT#3 as a transmitting RT, to a 73A-455 Module channel simulating RT#9 as a receiving RT, and to a 73A-455 Module channel simulating a Bus Controller in an RT-to-RT transfer of five words.

If only one or two of the three RT-to-RT participants are being simulated by a 73A-455 Module and the remainder by the actual hardware, then, of course, only those one or two channels would need to be programmed.

The programming of the 73A-455 Module as a Bus Controller or transmitting RT in an RT-to-RT transfer is straightforward. The programming of the 73A-455 Module as a receiving RT in an RT-to-RT transfer, however, requires some special consideration relating to the 73A-455 Module design.

In the following program for the receiving RT in lines 260 to 310, note that the receiving RT status word has been loaded in RT#3's buffer of the 73A-455 Module, even though the receiving RT is really at RT address 9. Also, the response time has been programmed to 130 microseconds rather than the normal 4 to 12 microseconds. This is because the 73A-455 programmed as an RT is designed to irrevocably start its response time counter at the occurrence of the first gap it sees following a command stream on the bus. This is the gap following the transmit RT command word from the bus controller. The 130 microsecond response time will, therefore, accommodate the time for the transmitting RT's status word and five data words plus some gap time before responding with the status word.

The reason for placing the status word in the buffer for RT#3 is that when a 73A-455 Module programmed as an RT does respond, it uses the last valid word with a command sync to select the RT buffer from which to transmit. Since the last valid command or status word is the status word from the transmitting RT (which has RT address 3 in the RT# bit locations), the RT's status word response must be in buffer 3.

Programming

The following program assumes the Bus Controller, transmitter RT, and receiving RT 73A-455 channels have IEEE-488 addresses 24, 25, and 26, respectively.

Lines 10 through 40 initialize the PC's IEEE-488 interface module as a system controller with an IEEE-488 address of decimal 21.

```
10   DEF SEG = &HC400
         Defines memory location of IBM PC IEEE-488 Interface Module.
20   SEND = 9 : INIT = 0 : ENTER = 21
         Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
30   PC.ADDRESS% = 21 : CONTROL% = 0
         Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a
         controller.
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADRBC% = 24
60   ADRXRT% = 25
70   ADRRRT% = 26
         Assign Bus Controller, transmit RT, and receive RT IEEE-488 addresses as 24, 25,
         and 26.
80   WRT$ = "K" + CHR$(13)
90   CALL SEND(ADRRT%, WRT$, STATUS%)
         Reset transmitting RT module.
100  WRT$ = "FR" + CHR$(13)
110  CALL SEND(ADRRT%, WRT$, STATUS%)
         Program module as an RT.
120  WRT$ = "B3,R99" + CHR$(13)
130  CALL SEND(ADRRT%, WRT$, STATUS%)
         Allocate a receive buffer at RT address 3.
140  WRT$ = "B3,T6" + CHR$(13)
150  CALL SEND(ADRRT%, WRT$, STATUS%)
         Allocate a transmit buffer of 6 words.
160  WRT$ = "D3,1,H,101800,1111,2222,3333,4444,5555:" + CHR$(13)
170  CALL SEND(ADRRT%, WRT$, STATUS%)
         Load transmit buffer with status word and 5 data words.
180  WRT$ = "T1" + CHR$(13)
190  CALL SEND(ADRRT%, WRT$, STATUS%)
         Trigger module to handle one message on bus.
200  WRT$ = "K" + CHR$(13)
210  CALL SEND(ADRRRT%, WRT$, STATUS%)
         Reset receiving RT module.
220  WRT$ = "FR" + CHR$(13)
230  CALL SEND(ADRRRT%, WRT$, STATUS%)
         Program module as an RT.
240  WRT$ = "R1,130" + CHR$(13)
250  CALL SEND(ADRRRT%, WRT$, STATUS%)
         Program a response time of 130 µsec.
260  WRT$ = "B3,R99" + CHR$(13)
270  CALL SEND(ADRRRT%, WRT$, STATUS%)
         Allocate a receive buffer at RT address 3.
280  WRT$ = "B3,T1" + CHR$(13)
290  CALL SEND(ADRRRT%, WRT$, STATUS%)
         Allocate a transmit buffer for 1 status word.
300  WRT$ = "D3,1,H,104800:" + CHR$(13)
```

```
310 CALL SEND(ADRRRT%, WRT$, STATUS%)
        Load transmit list with status word. The characters 48 define the status word to be
        from RT 9.
320 WRT$ = "T1" + CHR$(13)
330 CALL SEND(ADRRRT%, WRT$, STATUS%)
        Trigger module to handle one message on bus.
340 WRT$ = "K" + CHR$(13)
350 CALL SEND(ADRBC%, WRT$, STATUS%)
        Reset Bus Controller module.
360 WRT$ = "FC" + CHR$(13)
370 CALL SEND(ADRBC%, WRT$, STATUS%)
        Program module as bus controller.
380 WRT$ = "BS1" + CHR$(13)
390 CALL SEND(ADRBC%, WRT$, STATUS%)
        Allocate a message buffer size of 1.
400 WRT$ = "B3,R99" + CHR$(13)
410 CALL SEND(ADRBC%, WRT$, STATUS%)
        Allocate a receive buffer at RT address 3.
420 WRT$ = "B3,T2" + CHR$(13)
430 CALL SEND(ADRBC%, WRT$, STATUS%)
        Allocate transmit buffer for 2 words.
440 WRT$ = "S1,3" + CHR$(13)
450 CALL SEND(ADRBC%, WRT$, STATUS%)
        Specify message to come from transmit buffer #3.
460 WRT$ = "D3,1,H,104825, 101C25:" + CHR$(13)
470 CALL SEND(ADRBC%, WRT$, STATUS%)
        Load transmit list with 2 contiguous command words.
480 WRT$ = "T1" + CHR$(13)
490 CALL SEND(ADRBC%, WRT$, STATUS%)
        Trigger module to transmit RT-to-RT command on bus.
500 WRT$ = "A3,1,H" + CHR$(13)
510 CALL SEND(ADRBC%, WRT$, STATUS%)
        Program bus controller module to return receive buffer contents in hexadecimal.
520 PRINT ""
530 FOR I = 1 TO 9
540 RD$ = SPACE$ (255)
550 CALL ENTER (RD$, LENGTH%, ADRBC%, STATUS%):PRINT RD$
560 NEXT I
        Read and print 9 words.
570 PRINT " "
580 WRT$ = "A3,1,H" + CHR$(13)
590 CALL SEND(ADRXRT%, WRT$, STATUS%)
        Program transmitting RT to return received data.
600 FOR I = 1 TO 2
610 RD$ = SPACE$ (255)
620 CALL ENTER (RD$, LENGTH%, ADRXRT%, STATUS%):PRINT RD$
630 NEXT I
        Read and print 2 words.
640 PRINT " "
650 WRT$ = "A3,1,H" + CHR$(13)
660 CALL SEND(ADRRRT%, WRT$, STATUS%)
```

```
        Program receiving RT to return received data
670  FOR I = 1 TO 8
680  RD$ = SPACE$ (255)
690  CALL ENTER (RD$, LENGTH%, ADRRRT%, STATUS%):PRINT RD$
700  NEXT I
710  STOP
```

The following data will be returned from the bus controller receiver.

104825	First command word stuffed by 455 Module in receive buffer.
101800	Transmit RT status word
001111	Transmit RT data words
002222	
003333	
004444	
005555	
104800	Receive RT status word
0B0000	No more data

The following data will be returned from the transmitting RT receive buffer.

101C25	The second command word from the bus controller.
0B0000	No more data. An RT only collects command or status words with an RT address the same as the buffer numbers plus any data words following that command word.

The following data will be returned from the receiving RT receive buffer:

101C25	The second command word from the bus controller.
101800	The status word from the transmitting RT
001111	Data words
002222	
003333	
004444	
005555	
0B0000	No more data

An additional 73A-455 instrument channel programmed as a bus monitor would collect all nine words involved in the transaction.

RT-to-RT Timeout Test

A special requirement for RTs supporting RT-to-RT transfer capability is that a receiving RT time out when looking for a transmitting RT message occurring between 54 and 60 microseconds following the parity transition of the second command word in the bus controller RT-to-RT command sequence. This requirement is to prevent the receiving RT from getting hung up because of a malfunctioning transmitting RT. One channel can be used for this test as both the bus controller and transmitting RT, which responds more than 14 microseconds after the bus controller command sequence. The channel is programmed as a bus controller, and then programmed to simulate both devices.

Lines 10 through 40 initialize the PC's IEEE-488 interface module as a system controller with an IEEE-488 address of decimal 21.

```
10   DEF SEG = &HC400
         Defines memory location of IBM PC IEEE-488 Interface Module.
20   SEND = 9 : INIT = 0 : ENTER = 21
         Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
30   PC.ADDRESS% = 21 : CONTROL% = 0
         Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a
         controller.
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADR455% = 24
         Assign IEEE-488 address 24 to 73A-455 Module.
60   WRT$ = "K" + CHR$(13)
70   CALL SEND(ADR455%, WRT$, STATUS%)
         Reset module program as bus controller and transmitting RT.
80   WRT$ = "FC" + CHR$(13)
90   CALL SEND(ADR455%, WRT$, STATUS%)
100  WRT$ = "BS2" + CHR$(13)
110  CALL SEND(ADR455%, WRT$, STATUS%)
120  WRT$ = "B3,R99" + CHR$(13)
130  CALL SEND(ADR455%, WRT$, STATUS%)
140  WRT$ = "B3,T5" + CHR$(13)
150  CALL SEND(ADR455%, WRT$, STATUS%)
         Program module as a bus controller and allocate sequence, transmit, and receive
         buffers.
160  WRT$ = "S1,3:3,54" + CHR$(13)
170  CALL SEND(ADR455%, WRT$, STATUS%)
         Set interval between controller command and RT command and data to 54 µsec.
180  WRT$ = "D3,1,H,104822,101C22:101800,1111,2222:" + CHR$(13)
190  CALL SEND(ADR455%, WRT$, STATUS%)
         Program RT-toRT command words and transmitting RT message.
200  WRT$ = "T1" + CHR$(13)
210  CALL SEND(ADR455%, WRT$, STATUS%)
         Trigger sequence.
220  WRT$ = "A3,3,H" + CHR$(13)
230  CALL SEND(ADR455%, WRT$, STATUS%)
         Read third word in receive buffer.
240  RD$ = SPACE$ (255)
```

```
250  CALL ENTER (RD$, LENGTH%, ADR455%, STATUS%)
260  IF MID$(RD$,3,4)<>"4822":PRINT"CHANNEL TIMEOUT TOO SOON":GOTO 460
          If not receiving RT status, fail channel.
270  WRT$ = "S2,3,60:" + CHR$(13)
280  CALL SEND(ADR455%, WRT$, STATUS%)
290  WRT$ = "T1" + CHR$(13)
300  CALL SEND(ADR455%, WRT$, STATUS%)
          Reprogram interval to 60 µsec.
310  WRT$ = "A3,3,H" + CHR$(13)
320  CALL SEND(ADR455%, WRT$, STATUS%)
          Read third word in receive buffer.
330  RD$ = SPACE$ (255)
340  CALL ENTER (RD$, LENGTH%, ADR455%, STATUS%)
350  IF MID$(RD$,1,6)<>"0B0000":PRINT"CHANNEL TIMEOUT TOO LATE"
          If not a no-response, fail channel.
440  END
```

APPENDIX E - PERFORMANCE VERIFICATION

This procedure verifies the performance of the 73A-455 MIL-STD-1553 A/B Bus Simulator Modules. Perform the verification in your current VXIbus system if it meets the minimum requirements specified in the paragraph labeled *Required Equipment*. It is not necessary to complete the entire procedure if you are only interested in a specific performance area. However, the verification of some parameters rely on the correct operation of previously validated functions so it is best to follow the order presented.

Use the steps in this chapter to verify that the mainframe operates properly.

General Information and Conventions

The following conventions apply throughout this procedure:

- Each of the voltage and bit tests direct you to figures that help you visualize what the signal should look like. You will be referred to a different figure of a valid signal when the sample rate or voltage level changes.
- Programming of the 73A-455 assumes no particular interface. Refer to *Programming Examples in Basic* for a list of the ASC commands that need to be sent to the 73A-455. Form the commands properly for the interface that you use.
- This procedure checks one of two channels of the 73A-455, then instructs you to repeat the procedure for the other channel.

***NOTE**. Refer to the Command Syntax section of this manual for command protocol and syntax information.*

Prerequisites

The performance checks in this section are valid when the following requirements are met:

- The 73A-455 passes the power-on self test.
- All covers are in place and the 73A-455 is installed in an approved VXIbus mainframe according to the instructions in the *Installation* section of the Operating Manual.
- The 73A-455 warms up at least 20 minutes in an ambient environment as specified in the *Specifications* section of the Operating Manual.

Required Equipment

The following equipment is necessary to complete the performance verification checks:

- Digitizing oscilloscope with at least 500 MHz bandwidth, a sample frequency of 1 GHz, and a minimum of 2 channels.
- A platform to send commands to the 73A-455 and receive data back from the 73A-455.
- A cable to connect the direct coupled output of the 73A-455 from Direct A to Direct B. This cable will need to have a TNC Triax connector on each end and a 35 ± 0.1% Ω load across the bus high to bus low connection to simulate a 70 Ω 1553 bus load. Allow enough space to connect an oscilloscope probe on both ends of the resistor. Mark which side of the resistor is BUS+ and BUS–. Refer to Figure 455-7.
- One DD50S connector to monitor signals from the 73A-455.

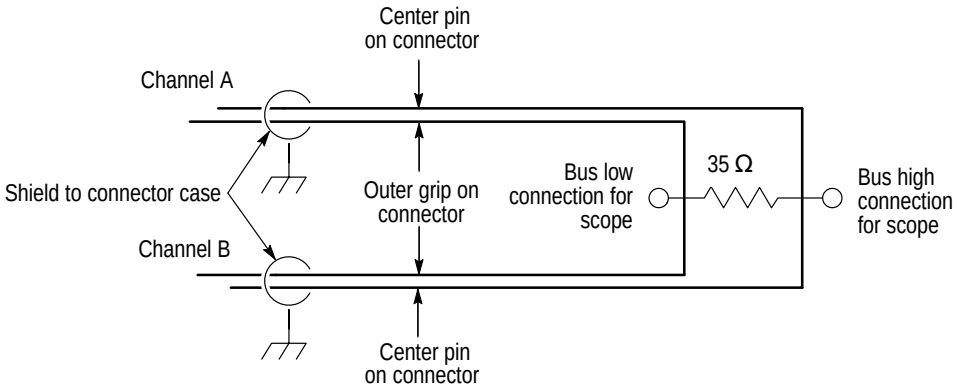


Figure 455-7: Cable Diagram

Performance Verification Check

Use the checks in this section to verify the performance of the 73A-455.

Verify Clock Stability

Follow the steps below to verify that the clock and dividers are working properly:

1. Connect channel 1 of the oscilloscope to S4 pin 39 (position identification output Bus A).

***NOTE**. Program the Bus A side of the 73A-455 module using the logical address.*

---

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   D0,1,H,300821;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Verify that the Bus A CTRL, PATT, and COMM lights are illuminated.

4. Measure the time on channel 1, between the falling edge of one pulse to the falling edge of the next pulse. A measurement of 70 µs ± 70 ns indicates that the clock and dividers are working properly. Refer to Figure 455-8.

5. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

6. Connect channel 1 of the oscilloscope to S4 pin 45 (position identification output Bus B).

7. Send the following commands to Bus B:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

BS1 <cr/lf>

S1,0,50;<cr/lf>

D0,1,H,300821;<cr/lf>

VT820,35<cr/lf>

T*<cr/lf>

8. Verify that the 73A-455 Bus B CTRL, PATT, and COMM lights are on.

9. Measure the time on channel 1 between the falling edge of one pulse to the falling edge of the next pulse. Refer to Figure 455-8 to verify a measurement of 70 µs ± 70 ns. This measurement indicates that the clock and dividers are working properly. .

10. Send the following command to the 73A-455 to make the transmitter quit and reset:

K<cr/lf>

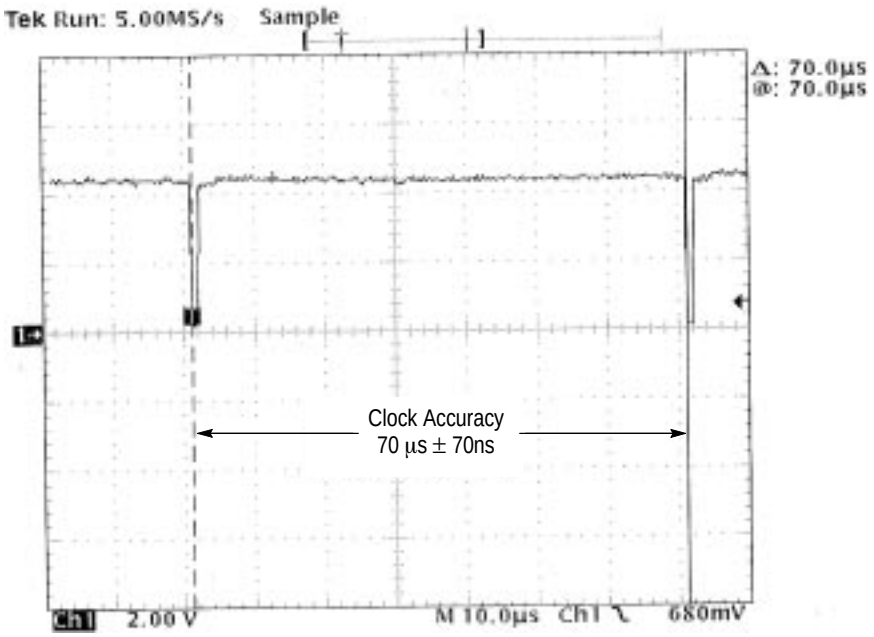


Figure 455-8: Clock Accuracy

Verify 1553 Bus Output Levels

Follow the steps below to verify that the 1553 bus output levels are accurate:

1. Connect one TNC Triax connector to the Direct A connector.
2. Connect a second TNC Triax connector to the Direct B connector.
3. Connect oscilloscope channel 1 to S4 pin 39. Connect channel 2 to BUS+ on the resistor.
4. Place the probe ground connection on the BUS– side of the resistor.
5. Set the oscilloscope to trigger off channel 1.

Ignore the overshoot and ringing on the peaks of the pulses when measuring the peak-to-peak amplitude of the 1553 message on channel 2. Refer to Figure 455-8 to verify the peak-to-peak measurement.

Amplitude Test, Volts Peak-to-Peak. Follow the steps below to verify the peak-to-peak voltage reading:

1. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   D0,1,H,300821;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

2. Measure the peak-to-peak amplitude. Verify that the reading is 8.20 V_{p-p} ± 300 mV. Refer to Figure 455-9.
3. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

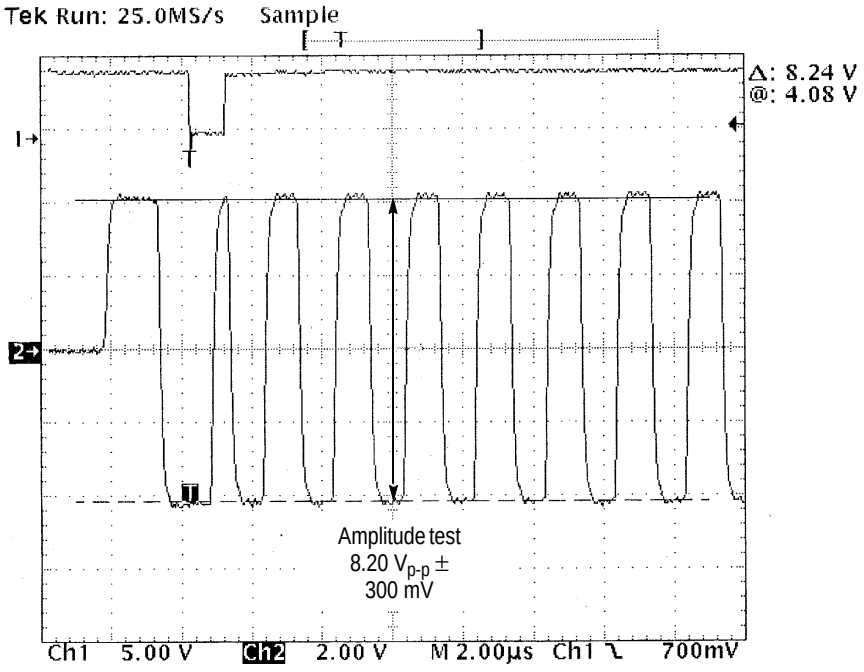


Figure 455-9: Amplitude Test, Volts Peak-to-Peak

Amplitude Test, Millivolt Peak-to-Peak. Follow the steps below to verify the peak-to-peak voltage reading:

1. Send the following commands to Bus A:

FC <cr/lf>

B0,T1 <cr/lf>

B0,R1 <cr/lf>

BS1 <cr/lf>

S1,0,50;<cr/lf>

D0,1,H,300821;<cr/lf>

VT020,35<cr/lf>

T*<cr/lf>

2. Measure the peak-to-peak amplitude of the 1553 message on channel 2. Refer to Figure 455-10 to verify that the measurement is 200 mV_{p-p} ± 300 mV.

3. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

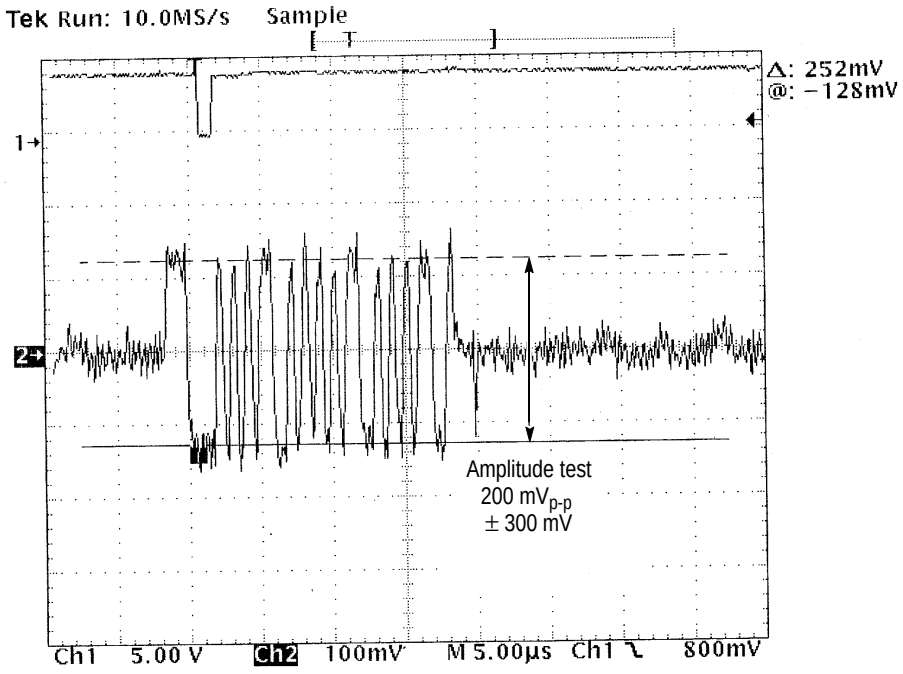


Figure 455-10: Amplitude Test, Millivolts Peak-to-Peak

Amplitude Test for Bus B. Follow the steps below to check the amplitude for Bus B.

1. Connect oscilloscope channel 1 to S4 pin 45.
2. Send the following commands to Bus B:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   D0,1,H,300821;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Measure the peak-to-peak amplitude of the 1553 message on channel 2. Verify that the reading is 8.20 V_{p-p} ± 300 mV. Refer to Figure 455-9.

4. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

5. Send the following commands to Bus B:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   D0,1,H,300821;<cr/lf>

   VT020,35<cr/lf>

   T*<cr/lf>

6. Measure the peak-to-peak amplitude of the 1553 message on channel 2. Refer to Figure 455-10 to verify that the reading is 200 mV ± 300 mV_{p-p}.

7. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

Error Injection Test

Follow the steps below to verify that there is no error in the injection transmission. Refer to Figure 455-11.

1. Connect one TNC Triax connector to the Direct A connector.

2. Connect a second TNC Triax connector to the Direct B connector.

3. Connect oscilloscope channel 1 to S4 pin 39 and channel 2 to BUS+ on the resistor.

4. Place the probe ground connection on the BUS– side of the resistor.

5. Set the oscilloscope to trigger off channel 1.

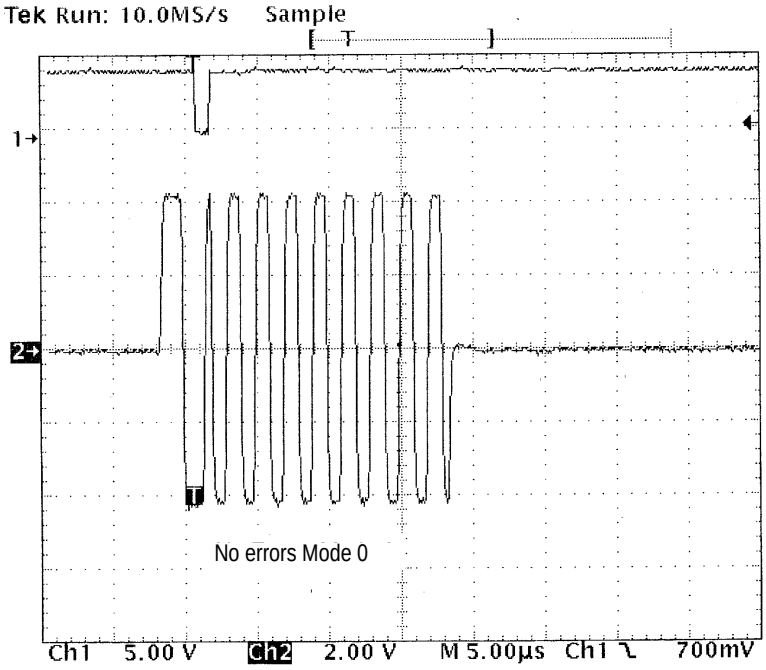


Figure 455-11: No Error Injection

Midsync Transition Error 500ns Early. Follow the steps below to generate a midsync transition reading:

1. Send the following commands to Bus A:

FC <cr/lf>

B0,T1 <cr/lf>

B0,R1 <cr/lf>

BS1 <cr/lf>

S1,0,50;<cr/lf>

M0<cr/lf>

D0,1,H,31AAAA;<cr/lf>

VT820,35<cr/lf>

T*<cr/lf>

2. Measure from the beginning of the sync to midsync. Verify that the reading is 1 µs ± 70 ns. Refer to Figure 455-12.

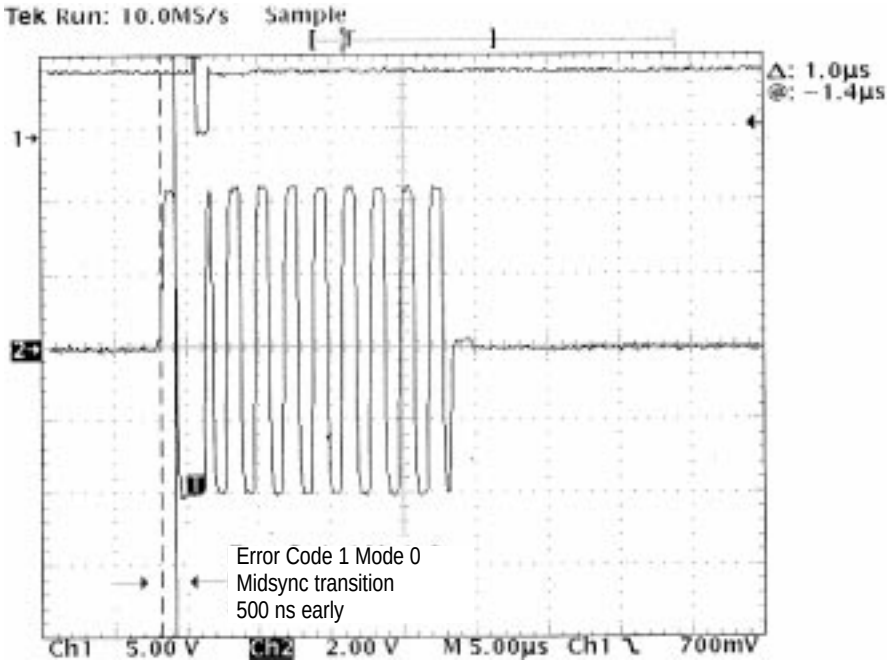


Figure 455-12: Midsync Transition 500 ns Early

Invalid Parity Error. Follow the steps below to generate an invalid parity error:

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,32AAAA;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Verify that the parity bit is the opposite of Figure 455-11 (no error injection transmission). Refer to Figure 455-13 for an example of an invalid parity.

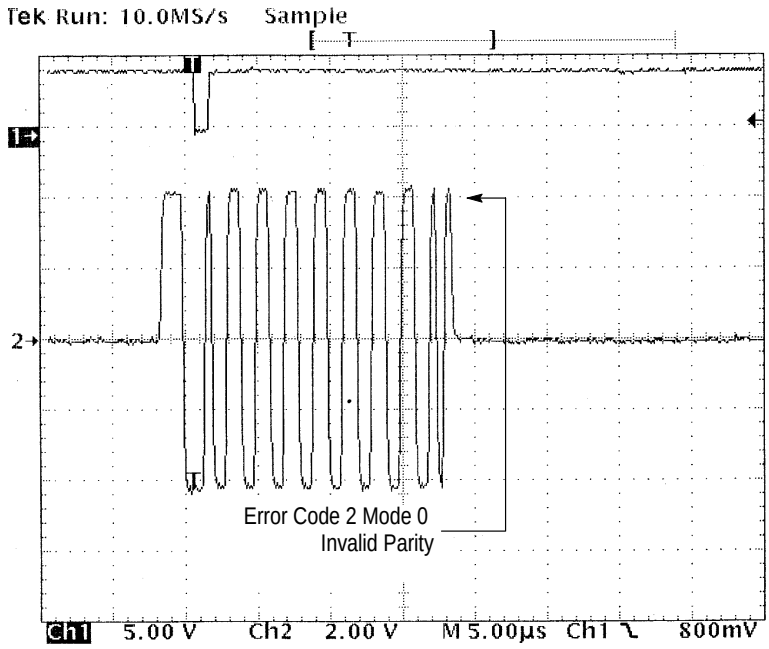


Figure 455-13: Invalid Parity

Manchester Error. Follow the steps below to generate a Manchester error:

NOTE. A Manchester error is when the bus is held high or low for a complete bus cycle (≥ 1 µs).

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

M0<cr/lf>

D0,1,H,33AAAA;<cr/lf>

VT820,35<cr/lf>

T*<cr/lf>

3. Compare Figure 455-14 (no Manchester error) to Figure 455-15 (with a Manchester error) to insure that there is a Manachester error.

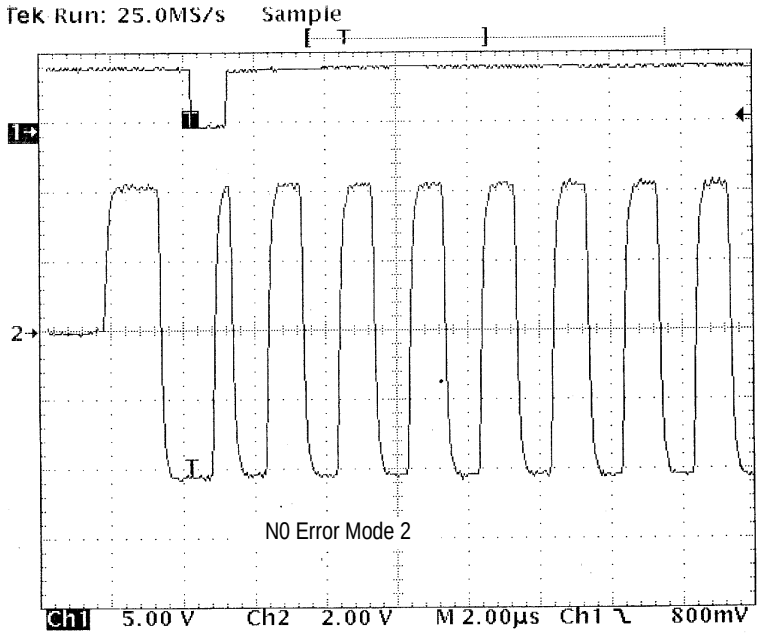


Figure 455-14: No Manchester Error

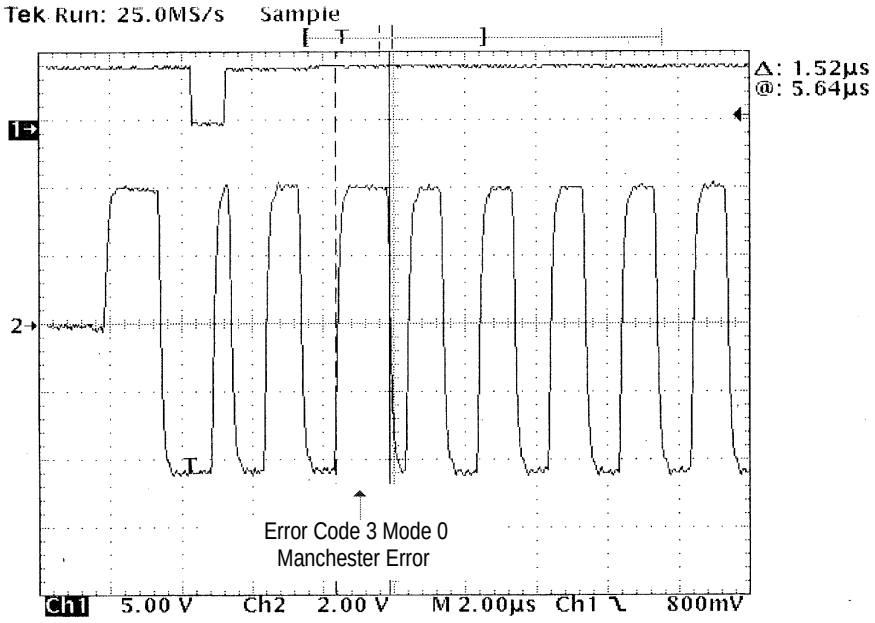


Figure 455-15: Manchester Error.

Sync Transition 500 ns Late. Follow the steps below to generate a sync transition error reading:

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,34AAAA;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

Refer to Figure 455-16 to verify a measured value is 2 µs ± 70 ns.

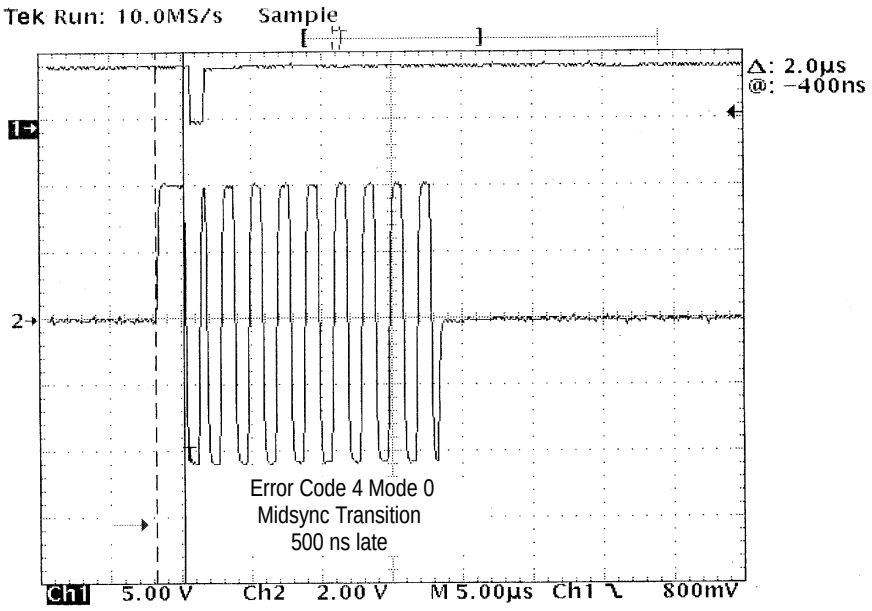


Figure 455-16: Midsync Transition 500 ns Late

17-bit Word Error. Follow the steps below to add one bit to the 16 bit word. Refer to Figure 455-17.

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,35AAAA;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Verify that an additional bit has been added.

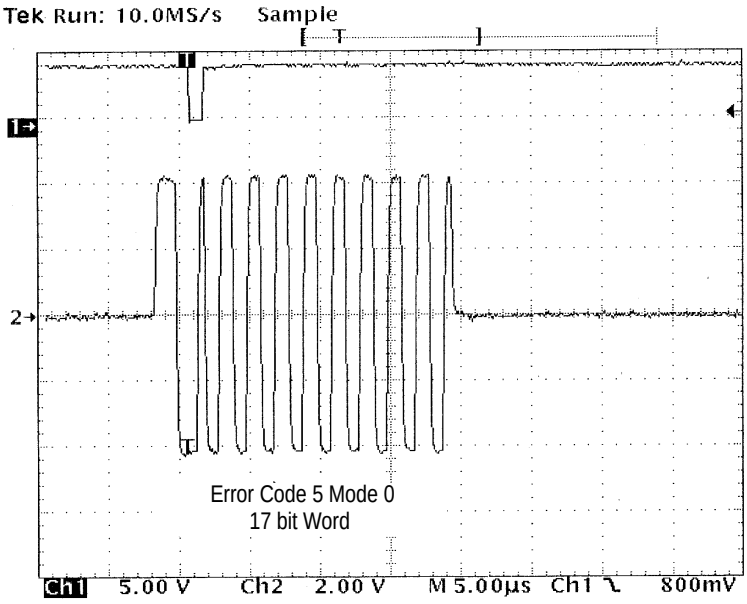


Figure 455-17: 17 bit Word

15-bit Word Error. Follow the steps below to subtract one bit from the 16 bit word. Refer to Figure 455-18.

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,36AAAA;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Verify that a bit has been removed.

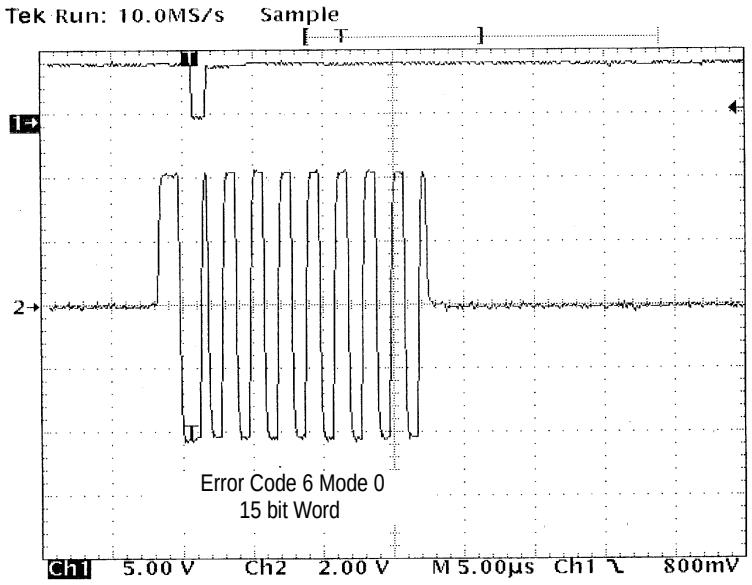


Figure 455-18: 15 bit Word

Dropped Bit Error. Follow the steps below to hold the reference level at 0.0 V for the bit transition time. Release the reference level for the next transition. Refer to Figure 455-19.

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,37AAAA;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Verify that a bit has dropped in the same position as Figure 455-19.

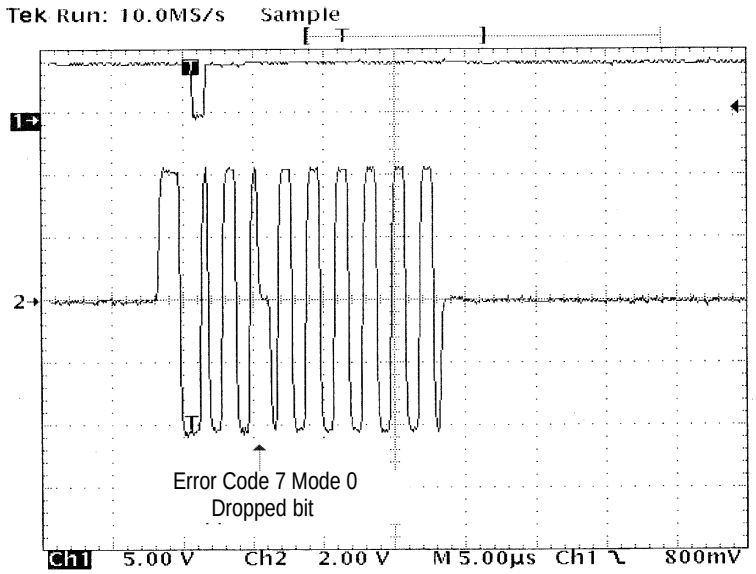


Figure 455-19: Dropped Bit

Dropped Bit on Position 16. Follow the steps below to check the ability of the 73A-455 to place a dropped bit on bit position 16. Refer to Figure 455-20.

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus A:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,37AAA0;<cr/lf>

   VT820,35<cr/lf>

   T*<cr/lf>

3. Verify that there is a dropped bit in position 16.

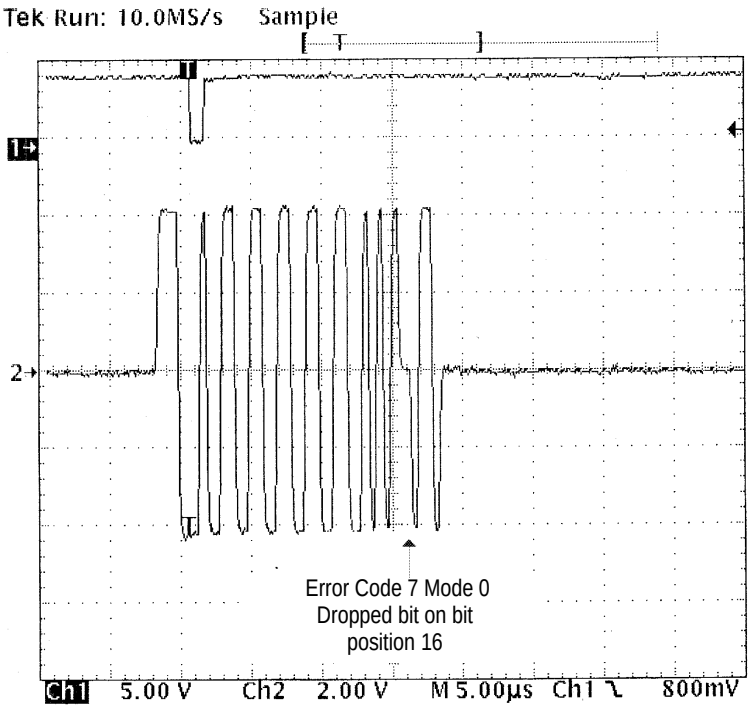


Figure 455-20: Dropped Bit on Position 16

Dropped Bit on Position 1. Follow the steps below to check the ability to place a dropped bit on bit position 1. Refer to Figure 455-21.

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus:

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M0<cr/lf>

   D0,1,H,37AAAE;<cr/lf>

3. Verify that there is a dropped bit in position one.

VT820,35<cr/lf>

T*<cr/lf>

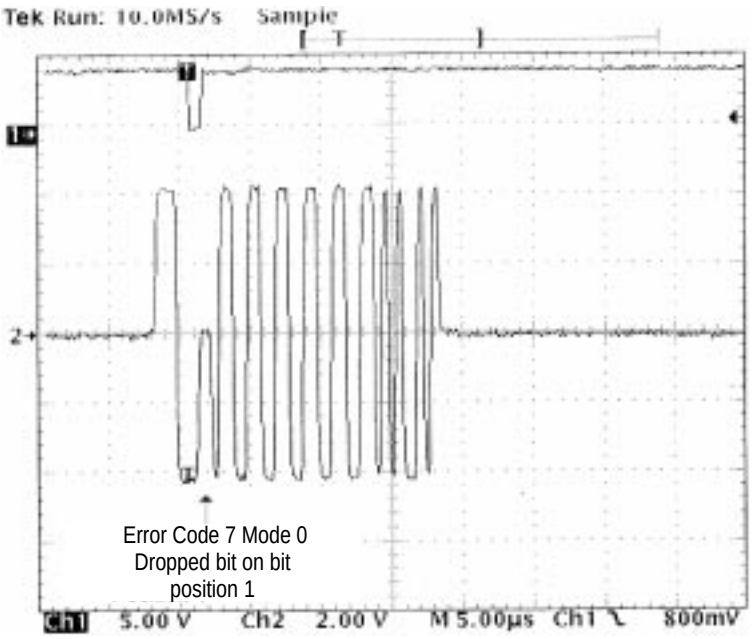


Figure 455-21: Dropped Bit on Position 1

Valid Midbit Transition Time. Follow the steps below to check for a valid midbit transition of 150 ns ± 70 ns.

1. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

2. Send the following commands to Bus:

   K <cr/lf>

   FC <cr/lf>

   B0,T1 <cr/lf>

   B0,R1 <cr/lf>

   BS1 <cr/lf>

   S1,0,50;<cr/lf>

   M1<cr/lf>

D0,1,H,33AAAD;<cr/lf>

VT820,35<cr/lf>

T*<cr/lf>

3. Verify that there is an invalid bit time.

Refer to Figure 455-22 for a valid midbit transition. Refer to Figure 455-23 for the invalid midbit transition.

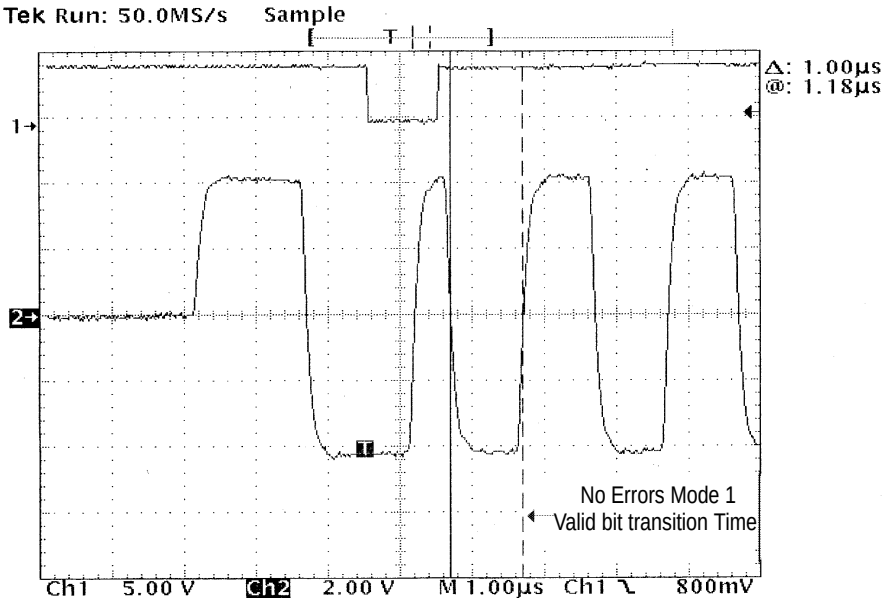


Figure 455-22: Valid Midbit Transition Time

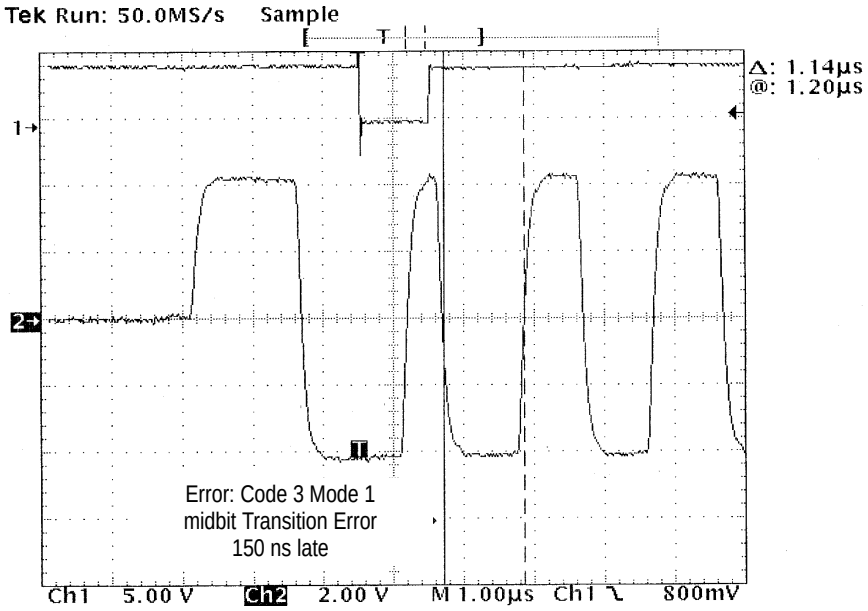


Figure 455-23: Invalid Midbit Transition

4. Send the following command to the 73A-455 to make the transmitter quit and reset:

   K<cr/lf>

This completes the transmitter testing for channel A of the 73A-455. Repeat the transmitter testing for channel B of the 73A-455. Begin with Error Injection Test on page 106.

The 1553 bus tester transmitter tests are complete if all tests are successful.

When you complete the transmitter testing for both channel A and channel B, proceed with the rest of the checks, beginning with Receiver Amplitude Test.

If problems are encountered, contact your Tektronix field office or representative for service assistance. For technical assistance with application questions, please contact the Measurement Business Customer Support Center at 1–800–835–9433 (800 TEK-WIDE), extension 2400.

Receiver Amplitude Test

Follow the steps below to verify the receiver amplitude:

1. Remove the channel 1 and channel 2 oscilloscope probes from the bus resistor.
2. Connect the bus cable between Direct A and Direct B connectors of the 73A-455.
3. Send the following commands to channel B Remote Terminal (RT):

   K<cr/lf>

   FR<cr/lf>

   B20,T3<cr/lf>

   B20,R3<cr/lf>

   D20,1,H,10A000,001111,00EEEE;<cr/lf>

   VT820,35<cr/lf>

   VR785<cr/lf>

   T1<cr/lf>

4. Send the following commands to channel A Bus Controller (BC):

   K<cr/lf>

   FC<cr/lf>

   B1,T1<cr/lf>

   B1,R5<cr/lf>

   BS1<cr/lf>

   S1,1,1000;<cr/lf>

   D1,1,H,10A422;<cr/lf>

   VT820,35<cr/lf>

   VR785<cr/lf>

   T1<cr/lf>

5. Wait approximately 100 μs before sending out any other commands.
6. Send the following commands to the BC:

   Q<cr/lf>

   A1,1,H<cr/lf>

7. Read back the following five words from the BC:

   10A422

   10A000

   001111

   00EEEE

   0B0000

   The first two bytes of each word may differ, but the last four bytes must match each of the above listed words.

8. Send the following commands to the RT:

   Q<cr/LF>

   A20,1,H<cr/lf>

9. Read back the following two words from the RT:

   10A422

   0B0000

   The first two bytes of each word may differ, but the last four bytes must match each of the above listed words.

10. Send the following commands to channel B:

    VR820<cr/lf>

    T1<cr/lf>

11. Send the following commands to channel A:

    VR820<cr/lf>

    T1<cr/lf>

12. Wait approximately 100 µs before sending out any other commands.

13. Send the following commands to the BC:

    Q<cr/lf>

    A1,1,H<cr/lf>

14. Read back the following word from the BC:

    0B0000

    The last four bytes should match the above word.

15. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

16. Read back the following word from the RT:

0B0000

The last four bytes should match the above word.

17. Send the following commands to channel B:

VT100,35<cr/lf>

VR50<cr/lf>

T1<cr/lf>

18. Send the following commands to channel A:

VT100,35<cr/lf>

VR50<cr/lf>

T1<cr/lf>

19. Wait approximately 100 µs before sending out any other commands.

20. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

21. Read back the following five words from the BC:

10A422

10A000

001111

00EEEE

0B0000

The first two bytes of each word may differ, but the last four bytes must match each of the above listed words.

22. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

23. Read back the following two words from the RT:

10A422

0B0000

The first two bytes of each word may differ, but the last four bytes must match each of the above listed words.

24. Send the following commands to channel B:

VT040,35<cr/lf>

T1<cr/lf>

25. Send the following commands to channel A:

VT040,35<cr/lf>

T1<cr/lf>

26. Wait approximately 100 µs before sending out any other commands.

27. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

28. Read back the following word from the BC:

0B0000

The first two bytes of each word may differ, but the last four bytes must match each of the above listed words.

29. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

30. Read back the following word from the RT:

0B0000

The first two bytes of each word may differ, but the last four bytes must match each of the above listed words.

This completes the Receiver Amplitude Test.

Receiver Error Detection Test

Follow the steps below to complete the Receiver Error Detection test:

1. Send the following commands to channel B:

   K<cr/lf>

   FR<cr/lf>

   B20,T3<cr/lf>

   B20,R3<cr/lf>

   D20,1,H,10A000,001111,01EEEE;<cr/lf>

   VT620,35<cr/lf>

   VR200<cr/lf>

   T1<cr/lf>

2. Send the following commands to channel A:

   K<cr/lf>

   FC<cr/lf>

   B1,T1<cr/lf>

   B1,R5<cr/lf>

   BS1<cr/lf>

   S1,1,1000;<cr/lf>

   D1,1,H,10A422;<cr/lf>

   VT620,35<cr/lf>

   VR200<cr/lf>

   T1<cr/lf>

3. Wait approximately 100 µs before sending out any other commands.

4. Send the following commands to the BC:

   Q<cr/lf>

   A1,1,H<cr/lf>

5. Read back the following five words from the BC:

   10A422

   10A000

   001111

   04EEEE

   0B0000

   Each word must match the above listed word.

6. Send the following commands to the RT:

   Q<cr/LF>

   A20,1,H<cr/lf>

7. Read back the following two words from the RT:

   10A422

   0B0000

   Each word must match the above listed word.

8. Send the following commands to channel B:

   D20,3,H,02EEEE;<cr/lf>

   T1<cr/lf>

9. Send the following commands to channel A:

   T1<cr/lf>

10. Wait approximately 100 µs before sending out any other commands.

11. Send the following commands to the BC:

    Q<cr/lf>

    A1,1,H<cr/lf>

12. Read back the following five words from the BC:

10A422

10A000

001111

02EEEE

0B0000

Each word must match the above listed word.

13. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

14. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

15. Send the following commands to channel B:

D20,3,H,03EEEE;<cr/lf>

T1<cr/lf>

16. Send the following commands to channel A:

T1<cr/lf>

17. Wait approximately 100 µs before sending out any other commands.

18. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

19. Read back the following five words from the BC:

10A422

10A000

001111

03EEEE

0B0000

Each word must match the above listed word.

20. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

21. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

22. Send the following commands to channel B:

D20,3,H,04EEEE;<cr/lf>

T1<cr/lf>

23. Send the following commands to channel A:

T1<cr/lf>

24. Wait approximately 100 µs before sending out any other commands.

25. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

26. Read back the following five words from the BC:

10A422

10A000

001111

04EEEE

0B0000

Each word must match the above listed word.

27. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

28. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

29. Send the following commands to channel B:

D20,2,H,051111,00EEEE;<cr/lf>

T1<cr/lf>

30. Send the following commands to channel A:

T1<cr/lf>

31. Wait approximately 100 µs before sending out any other commands.

32. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

33. Read back the following five words from the BC:

10A422

10A000

001111

05EEEE

0B0000

Each word must match the above listed word.

34. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

35. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

36. Send the following commands to channel B:

D20,2,H,001111,06EEEE;<cr/lf>

T1<cr/lf>

37. Send the following commands to channel A:

T1<cr/lf>

38. Wait approximately 100 µs before sending out any other commands.

39. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

40. Read back the following five words from the BC. This requires five readbacks of eight bytes each.

10A422

10A000

001111

06EEEE

0B0000

Each word must match the above listed word.

41. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

42. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

43. Send the following commands to channel B:

D20,3,H,072222;<cr/lf>

T1<cr/lf>

44. Send the following commands to channel A:

T1<cr/lf>

45. Wait approximately 100 µs before sending out any other commands.

46. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

47. Read back the following five words from the BC:

10A422

10A000

001111

072222

0B0000

Each word must match the above listed word.

48. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

49. Read back the following 2words from the RT:

10A422

0B0000

Each word must match the above listed word.

50. Send the following commands to channel B:

BR1<cr/lf>

R1,5<cr/lf>

D20,3,H,00EEEE;<cr/lf>

T1<cr/lf>

51. Send the following commands to channel A:

G4<cr/lf>

T1<cr/lf>

52. Wait approximately 100 µs before sending out any other commands.

53. Send the following commands to the BC:

Q<cr/lf>

A1,1,H<cr/lf>

54. Read back the following five words from the BC:

10A422

11A000

011111

01EEEE

0B0000

Each word must match the above listed word.

55. Send the following commands to the RT:

Q<cr/LF>

A20,1,H<cr/lf>

56. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

57. Send the following commands to channel B:

BR1<cr/lf>

R1,4<cr/lf>

D20,3,H,00EEEE;<cr/lf>

T1<cr/lf>

58. Send the following commands to channel A:

G5<cr/lf>

D1,1,H,10A420;<cr/lf>

T1<cr/lf>

59. Wait approximately 100 μs before sending out any other commands.

60. Send the following commands to the BC:

Q<cr/lf>

A1,1,HF<cr/lf>

61. Read back the following five words from the BC:

19A420

10A000

001111

00EEEE or 0CEEEE

0B0000

Each word must match the above listed word.

62. Send the following commands to the RT:

Q<cr/LF>

A20,1,HF<cr/lf>

63. Read back the following two words from the RT:

10A422

0B0000

Each word must match the above listed word.

64. Repeat the *Receiver Error Detection Test* on page 120**,** reversing the function of the 73A-455 by making channel A the RT and channel B the BC.

The receiver tests are complete if all tests are successful.

Memory and CPU Test

Follow the steps below to verify the performance of the memory and CPU:

1. Send the following command to channel A:

   TEST<cr/lf>

2. Wait until all of the lights on channel A of the 73A-455 module have quit blinking.

3. Verify the 73A-455 displays the following message:

   OK, Vx.x

***NOTE**. Vx.x indicates the version and revision level of the firmware.*

If the above message is received, then there are no errors in the memory or CPU.

4. Repeat the memory and CPU test for the channel B.

If all performance checks in this section are verified, then the 73A-455 is operational.

If problems are encountered, contact your Tektronix field office or representative for service assistance. For technical assistance with application questions, please contact the Measurement Business Customer Support Center at 1-800-835-9433 (800 TEK-WIDE), extension 2400.

Appendix F
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

User-Replaceable Parts

Part Description	Part Number
User Manual	070-9136-XX
Label, Tek CDS	950-0626-00
Label, VXI	950-0627-00
Fuse, Micro 2 Amp 125 V Fast	159-0128-00
Fuse, Sub-min 7 Amp 125 Fast	159-0146-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-1343-00
Screw, Phillips Metric 2.5 × 5 CSK	950-3885-00
Screw, Phillips Metric 2.5 × 10 CSK Oval	950-1081-00
Screw, Phillips 2.5 MM × 16 MM 90 Deg CSK	950-5467-00
Screw, Phillips 2.5 MM × 20 MM 90 Deg CSK	211-0868-00

Appendix G
Option 2N

Option 2N to the 73A–455 MIL-STD-1553A/B Bus Simulator Module modifies the front panel connections on both MIL-STD-1553 channels to provide a higher input impedance at 1 MHz on the transformer coupled outputs.

To do this,

the direct-coupled outputs are disconnected,

the transformer-coupled connections to the D connector are disconnected, and

the transformer-coupled connections are wired point-to-point to the on-module transformer (they no longer use PC board traces).

The unit is tested at the factory at 1 MHz with a single-ended impedance measurement to be greater than 950 Ω. This means that if you make a floating differential impedance measurement, it will provide a differential input impedance greater than 1000 Ω.

Operational Changes: Transformer-coupled only.

Programming Changes: None.

Specification Changes: See above regarding input impedance.